Features

- ISO 11898-2:2024 parameter set A-C, SAE J2284-1 to SAE J2284-5 and SAE J1939-14 compliant with wake-up pattern wake-up
- CAN FD Signal Improvement Capability (SIC) according to ISO 11898-2:2024 to reduce ringing on bus signal
- Data rate up to 8 Mbps
- Fault voltage up to ±42 V for bus pins
- Integrated ESD and Surge Transient Voltage Suppressor (TVS) for bus pins
- TVS protection Immunities for bus terminals:
  ±8 kV IEC 61000-4-2, Contact Discharge
  ±8 kV SAE J2962-2:2019, Contact Discharge
  ±15 kV SAE J2962-2:2019, Air Discharge
- HBM ±5 kV ESD protection for all pins
- HBM ±8 kV ESD protection for bus pins
- MM ±400 V ESD protection for all pins
- High CDM protection up to ±800 V for all pins
- Latch up immunity up to ±400 mA for all pins
- High IEC 61000-4-4 Electrical Fast Transient (EFT) coupling immunity for bus pins under communication
- Capability to withstand ISO 7637-2 standard pulses 1, 2a, 3a and 3b
- Capability for both low ElectroMagnetic Emission (EME) and high ElectroMagnetic Immunity (EMI)
- Low standby current (8 μA, typical) for power saving
- V_{IO} input allows for direct interfacing with 1.8 V to 5 V microcontrollers
- Ideal passive behavior to CAN bus with supply power off
- Transmit Data (TXD) dominant time-out function
- Undervoltage detection on the pins of V_{CC} and V_{IO} power
- Current-limitation and thermal shutdown for the driver design
- AEC-Q100 qualified

Applications

- Automotive Electronics
- Industrial Control and Instrumentation Networks
- Motor Control
- Battery Control

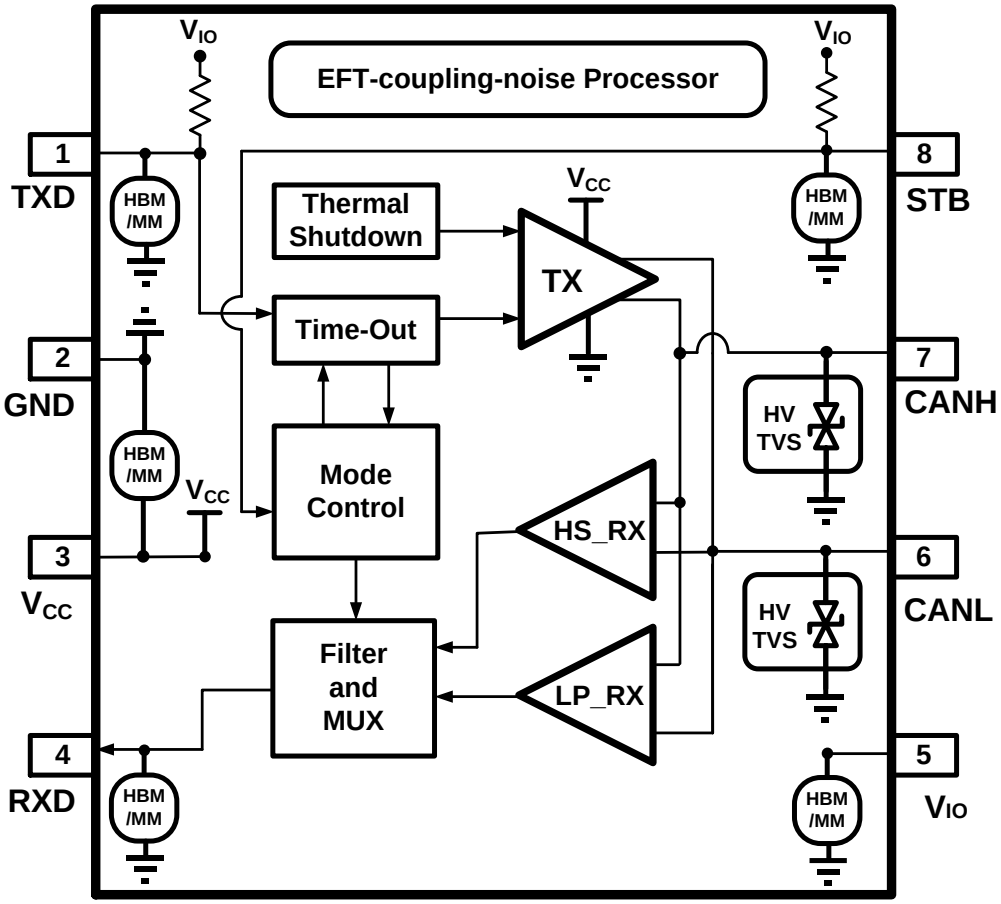
Description

The AZKN9325P is a ±8 kV IEC 61000-4-2 protected high speed Controller Area Network (CAN) transceiver IC. It serves as an interface between a CAN protocol controller (MCU) and the physical two-wire CAN bus. This device operates at 5 V power supply and is fully compliant with ISO 11898-2:2024 standard for CAN FD application. The AZKN9325P features CAN signal improvement capability, which is described in ISO 11898-2:2024 parameter set C. With signal improvement capability, the AZKN9325P can reduce signal ringing while bus is in a dominant-recessive transition, making more stable communication in complex network topologies. Furthermore, the bit timing symmetry of the AZKN9325P is much tighter and the data rate can up to 8 Mbps. The AZKN9325P has the capabilities of both the ±12 V common mode range of the receiver and the low EME of the transmitter, which has been patented as the Amazing's intellectual property. Moreover, the whole-chip design of the AZKN9325P can sustain high EFT coupling under communication.

The AZKN9325P is a robust CAN transceiver, which features ±42 V fault protection to sustain the DC short voltage on the bus pins. In addition, the whole-chip ESD protection immunity reaches HBM ±5 kV, MM ±400 V and CDM ±800 V, which is satisfied to withstand the ESD zapping under the worst manufacture environment.

The AZKN9325P is pin-compatible to 8-pin CAN FD transceivers, such as AZKN9125P, allowing the simple replacement to existing application

Functional Block of AZKN9325P



Thermal Characteristics

PARAMETER	SYMBOL	CONDITIONS	Value	UNIT
Thermal resistance from virtual junction to ambient	θ_{JA}[1]	P_H = 167 mW under the air flow rate = 0 m/s in the ambient temperature [2]	109.45	°C/W

[1] The thermal resistance between virtual junction and ambient is $\theta_{JA} = (T_J - T_{AMB})/P_H$, where T_J is the virtual junction temperature and T_{AMB} is the ambient temperature under the power dissipation of P_H.

[2] According to JEDEC JESD51-2 and JESD51-7 at natural convection on 2s2p board with two inner copper layers (Power/Ground thickness: 35 μm; Signal thickness: 70 μm).

Absolute Maximum Ratings [1]

PARAMETER	SYMBOL	MIN	MAX	UNIT
DC voltage on CANH, CANL	V_{CANH},V_{CANL}	-42	+42	V
DC voltage between pin CANH and pin CANL	$V_{(CANH-CANL)}$	-50	+50	V
DC voltage on all other pins	V_X	-0.3	+7	V
Transient voltage on pins CANH and CANL For ISO 7637-2 pulse 1 [2]	V_{trt1}	-100	-	V
Transient voltage on pins CANH and CANL For ISO 7637-2 pulse 2a [2]	V_{trt2a}	-	+75	V
Transient voltage on pins CANH and CANL For ISO 7637-2 pulse 3a [2]	V_{trt3a}	-150	-	V
Transient voltage on pins CANH and CANL For ISO 7637-2 pulse 3b [2]	V_{trt3b}	-	+100	V
System-level ESD (IEC 61000-4-2, Contact Discharge) -- at pins CANH, CANL	$V_{ESD(contact)}$	-8	+8	kV
System-level ESD (SAE J2962-2:2019, Powered Contact Discharge) -- at pins CANH, CANL				
System-level ESD (SAE J2962-2:2019, Powered Air Discharge) -- at pins CANH, CANL	$V_{ESD(air)}$	-15	+15	kV
HBM ESD (Human Body Model; 100 pF; 1.5 kΩ) -- at any pins [3]	V_{HBM}	-5	+5	kV
HBM ESD (Human Body Model; 100 pF; 1.5 kΩ) -- at pins CANH, CANL [3]	V_{HBM}	-8	+8	kV
MM ESD (Machine Model; 200 pF) -- at any pins [4]	V_{MM}	-400	+400	V
CDM ESD (Charged Device Model; field induced charge) -- at any pins [5]	V_{CDM}	-800	+800	V
Virtual junction temperature	T_J	-40	+150	°C
Storage temperature	T_{STO}	-55	+150	°C

[1] Stresses listed above may cause permanent damage to the device under “Maximum Ratings”. This is a stress rating only and functional operation of the device at those or other conditions above those indicated in the operational listings of this specification are not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

[2] Verified by thirty-party to ensure both CANH and CANL can withstand ISO 7637-2 automotive transient test pulses 1, 2a, 3a and 3b. The DUT is evaluated by the DCC method with coupling capacitance of 1nF connected between the pulse source and the cable of CANH and CANL respectively, which is shown in Figure 8.

[3] Verified by thirty-party referred to AEC-Q100-002

[4] Verified by thirty-party referred to AEC-Q100-003

[5] Verified by thirty-party referred to AEC-Q100-011

DC Electrical Characteristics

(V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.7 V to 5.5 V; T_{AMB} = -40 °C to +125 °C; R_L = 60 Ω unless otherwise noted. Typical values are at V_{CC} = 5 V; V_{IO} = 3.3 V and T_{AMB} = 25 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Internal Supply : V_{CC}						
Supply voltage	V_{CC}		4.5	-	5.5	V
Undervoltage detection voltage on pin V_{CC}	$V_{uvd(VCC)}$		3.5	4.0	4.5	V
Supply current	I_{CC}	Standby mode				
		$V_{TXD} = V_{IO}$	-	-	2	µA
		Normal mode				
		Recessive; $V_{TXD} = V_{IO}$	-	7	12	mA
		Dominant; $V_{TXD} = 0$ V; $t < t_{to(dom)TXD}$	20	40	70	mA
		Dominant; $V_{TXD} = 0$ V; Short circuit on bus lines; -3 V < ($V_{CANH} = V_{CANL}$) < +40 V	-	-	125	mA
Internal Supply : V_{IO}						
Supply voltage on pin V_{IO}	V_{IO}		1.7	-	5.5	V
Undervoltage detection voltage on pin V_{IO}	$V_{uvd(VIO)}$		-	1.4	1.7	V
Supply current	I_{IO}	Standby mode				
		$V_{TXD} = V_{IO}$	-	8	20	µA
		Normal mode				
		Recessive; $V_{TXD} = V_{IO}$	-	150	460	µA
		Dominant; $V_{TXD} = 0$V	-	250	760	µA
Bus Lines : CANH and CANL						
Dominant output voltage	$V_{O(dom)}$	Normal mode; V_{TXD} = 0 V; $t < t_{to(dom)TXD}$; V_{CC} = 4.75 V to 5.25 V				
		pin CANH; RL = 50 Ω to 65 Ω	2.89	3.5	4.26	V
		pin CANL; RL = 50 Ω to 65 Ω	0.77	1.5	2.13	V
Common mode voltage step	$V_{cm(step)}$	[2] [3] [4]	-150	-	+150	mV
Peak-to-peak common mode voltage	$V_{cm(p-p)}$	[2] [3] [4]	-300	-	+300	mV

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Transmitter voltage symmetry	V_{TXsym}	$V_{TXsym} = V_{CANH} + V_{CANL}$; [2] f_{TXD} = 250 kHz,1 MHz or 2.5 MHz; [3] C_{SPLIT} = 4.7 nF	0.9V_{CC}	-	1.1V_{CC}	V
Bus differential output voltage	$V_{O(dif)bus}$	Normal mode; V_{TXD} = 0 V; t < $t_{to(dom)TXD}$; V_{CC} = 4.75 V to 5.25 V				
		R_L = 50 Ω to 65 Ω	1.5	-	2.75	V
		R_L = 45 Ω to 70 Ω	1.4	-	3.3	V
		R_L = 2240 Ω [2]	1.5	-	5	V
		recessive; no load				
		Normal mode; V_{TXD} = V_{IO}	-50	-	+50	mV
		Standby mode	-0.2	-	+0.2	V
Recessive output voltage	$V_{O(rec)}$	Normal mode; V_{TXD} = V_{IO}; no load	2	0.5V_{CC}	3	V
		Normal mode; V_{TXD} = V_{IO}; R_L = 60 Ω	2.2	0.5V_{CC}	2.8	V
		Standby mode; no load	-0.1	-	+0.1	V
Receiver recessive voltage	$V_{rec(RX)}$	$V_{CM(CAN)}$ = -12 V to +12 V [1]				
		Normal mode	-4	-	0.5	V
		Standby mode	-4	-	0.4	V
Receiver dominant voltage	$V_{dom(RX)}$	$V_{CM(CAN)}$ = -12 V to +12 V [1]				
		Normal mode	0.9	-	9	V
		Standby mode	1.15	-	9	V
Differential receiver threshold voltage	$V_{th(RX)dif}$	$V_{CM(CAN)}$ = -12 V to +12 V [1]				
		Normal mode	0.5	0.7	0.9	V
		Standby mode	0.4	0.78	1.15	V
Differential receiver hysteresis voltage	$V_{hys(RX)dif}$	$V_{CM(CAN)}$ = -12 V to +12 V; [1] Normal mode	-	100	-	mV
Short-circuit output current	$I_{O(SC)dom}$	Normal mode; V_{TXD} = 0 V, V_{IO} or 250 kHz, 2.5 MHz square wave				
		Pin CANH; V_{CANH} = -15 V to 40 V; CANL = open	-115	-	-	mA
		Pin CANL; V_{CANL} = -15 V to 40 V; CANH = open	-	-	115	mA
Recessive short-circuit output current	$I_{O(SC)rec}$	Normal mode; V_{TXD} = V_{IO}; t > $t_{d(TXD-buspasrec)start}$; V_{CANH} = V_{CANL} = -27 V to +32 V	-3	-	+3	mA
Leakage current	I_L	V_{CC} = V_{IO} = 0 V or V_{CC} = V_{IO} = shorted to ground via 47 kΩ; V_{CANH} = V_{CANL} = 5 V	-10	-	+10	μA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input resistance	R_i	Passive recessive; -2 V ≦ V_{CANH} ≦ +7 V; -2 V ≦ V_{CANL} ≦ +7 V	25	40	50	kΩ
Input resistance deviation	ΔR_i	Passive recessive; 0 V ≦ V_{CANH} ≦ +5 V; 0 V ≦ V_{CANL} ≦ +5 V	-3	-	+3	%
Differential input resistance	$R_{i(dif)}$	Passive recessive; -2 V ≦ V_{CANH} ≦ +7 V; -2 V ≦ V_{CANL} ≦ +7 V	50	80	100	kΩ
Common-mode input capacitance	$C_{i(cm)}$	[2]	-	-	30	pF
Differential input capacitance	$C_{i(dif)}$	[2]	-	-	15	pF
Dominant phase input resistance	$R_{i(dom)}$	Bus dominant; TXD = 0 V; STB = 0 V	-	20	-	Ω
Dominant phase differential input resistance	$R_{i(dif)dom}$	$R_{i(dif)dom} = R_{i(dom)CANH} + R_{i(dom)CANL}$	-	40	-	Ω
Active recessive phase input resistance	$R_{i(actrec)}$	Bus dominant-to-recessive transition; V_{CC} = 4.75 V to 5.25 V; 1.5 V ≦ V_{CANH} ≦ V_{CC} - 1.5 V; 1.5 V ≦ V_{CANL} ≦ V_{CC} - 1.5 V	37.5	-	66.5	Ω
Active recessive phase differential input resistance	$R_{i(dif)actrec}$	$R_{i(dif)actrec} = R_{i(actrec)CANH} + R_{i(actrec)CANL}$	75	-	133	Ω
Temperature Protection						
Shutdown temperature	$T_{J(sd)}$	[2]	-	190	-	°C
Standby Mode Control Input : STB						
High-level input voltage	V_{IH}		$0.7V_{IO}$	-	V_{IO}+0.3	V
Low-level input voltage	V_{IL}		-0.3	-	$+0.3V_{IO}$	V
Hysteresis voltage	$V_{(hys)STB}$		50	-	-	mV
Pull-up resistance	R_{pu}		20	-	80	kΩ
Input capacitance	C_i	[2]	-	-	10	pF
Transmit Data Input : TXD						
High-level input voltage	V_{IH}		$0.7V_{IO}$	-	V_{IO}+0.3	V
Low-level input voltage	V_{IL}		-0.3	-	$+0.3V_{IO}$	V
Hysteresis voltage	$V_{(hys)TXD}$		50	-	-	mV
Pull-up resistance	R_{pu}		20	-	80	kΩ
Input capacitance	C_i	[2]	-	-	10	pF
Receive Data Output : RXD						
High-level output current	I_{OH}	V_{RXD} = V_{IO} - 0.4 V	-10	-	-1	mA
Low-level output current	I_{OL}	V_{RXD} = 0.4 V; bus dominant	1	-	10	mA

[1] $V_{CM(CAN)}$ is the common mode voltage of CANH and CANL.

[2] Not tested in production; guaranteed by design.

[3] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Figure 9.

[4] See Figure 3.

Switching Characteristics

(V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.7 V to 5.5 V; T_{AMB} = -40 °C to + 125 °C; R_L = 60 Ω unless otherwise noted. Typical values are at V_{CC} = 5 V; V_{IO} = 3.3 V and T_{AMB} = 25 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Transceiver timing according to ISO 11898-2:2024; V_{CC} = 4.5 V to 5.5 V; see Figure 1 and Figure 7						
Propagation delay from TXD to RXD	$t_{PD(TXD-RXD)}$	Normal mode	-	-	255	ns
Transceiver timing according to ISO 11898-2:2024; V_{CC} = 4.75 V to 5.25 V; see Figure 1 , Figure 7 and Figure 11						
Delay time from TXD to bus dominant	$t_{d(TXD-busdom)}$	Normal mode	-	-	80	ns
Delay time from TXD to bus recessive	$t_{d(TXD-busrec)}$	Normal mode	-	-	80	ns
Delay time from bus dominant to RXD	$t_{d(busdom-RXD)}$	Normal mode	-	-	110	ns
Delay time from bus recessive to RXD	$t_{d(busrec-RXD)}$	Normal mode	-	-	110	ns
Propagation delay from TXD to RXD	$t_{PD(TXD-RXD)}$	Normal mode	-	-	190	ns
Delay time from TXD to bus active recessive start	$t_{d(TXD-busactrec)start}$	Normal mode [5] [6]	-	-	120	ns
Delay time from TXD to bus active recessive end	$t_{d(TXD-busactrec)end}$	Normal mode [5] [6]	355	-	-	ns
Delay time from TXD to bus passive recessive start	$t_{d(TXD-buspasrec)start}$	Normal mode [5] [6]	-	-	530	ns
CAN FD timing according to ISO 11898-2:2024 parameter set C ($t_{bit(TXD)}$ ≥ 125 ns, up to 8 Mbps); VCC = 4.75 V to 5.25 V; see Figure 1 and Figure 7						
Transmitted recessive bit width deviation	$\Delta t_{bit(Bus)}$	$\Delta t_{bit(Bus)}$ = $t_{bit(Bus)}$ - $t_{bit(TXD)}$	-10	-	+10	ns
Receiver timing symmetry	Δt_{Rec}	Δt_{Rec} = $t_{bit(RXD)}$ - $t_{bit(Bus)}$	-20	-	+15	ns
Received recessive bit width deviation	$\Delta t_{bit(RXD)}$	$\Delta t_{bit(RXD)}$ = $t_{bit(RXD)}$ - $t_{bit(TXD)}$	-30	-	+20	ns
CAN FD timing ($t_{bit(TXD)}$ ≥ 200 ns, up to 5 Mbps); VCC = 4.5 V to 5.5 V; see Figure 1 and Figure 7						
Transmitted recessive bit width deviation	$\Delta t_{bit(Bus)}$	$\Delta t_{bit(Bus)}$ = $t_{bit(Bus)}$ - $t_{bit(TXD)}$	-30	-	+30	ns
Receiver timing symmetry	Δt_{Rec}	Δt_{Rec} = $t_{bit(RXD)}$ - $t_{bit(Bus)}$	-45	-	+15	ns
Received recessive bit width deviation	$\Delta t_{bit(RXD)}$	$\Delta t_{bit(RXD)}$ = $t_{bit(RXD)}$ - $t_{bit(TXD)}$	-50	-	+40	ns
Dominant Time-out Time; Pin TXD						
TXD dominant time-out time	$t_{to(dom)TXD}$	Normal mode; V_{TXD} = 0 V	0.8	2.3	9	ms
Bus Wake-up Times; Pins CANH and CANL						
Bus dominant wake-up time	$t_{wake(busdom)}$	Standby mode [2]	0.5	-	1.8	µs
Bus recessive wake-up time	$t_{wake(busrec)}$	Standby mode [2]	0.5	-	1.8	µs
Bus wake-up time-out time	$t_{to(wake)bus}$	Standby mode [2]	0.8	-	9	ms
Bus wake-up filter time	$t_{fltr(wake)bus}$	Standby mode [2]	0.5	-	1.8	µs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Mode Transition Times						
Mode change transition time	$t_{t(moch)}$	[3]	-	-	50	µs
Start-up time	$t_{startup}$	[4][6]	-	-	1.5	ms
IO Filter Time; Pin STB						
STB filter time	$t_{fltr(STB)}$		0.5	-	2.5	µs
Undervoltage Detection Times; Pins V_{CC} and V_{IO}						
Undervoltage detection time on pin V_{CC}	$t_{det(uv)VCC}$	[4][6]	-	-	30	µs
Undervoltage recovery time on pin V_{CC}	$t_{rec(uv)VCC}$	[4][6]	-	-	50	µs
Undervoltage detection time on pin V_{IO}	$t_{det(uv)VIO}$	[4][6]	-	-	30	µs

[1] See Figure 2.

[2] See Figure 4.

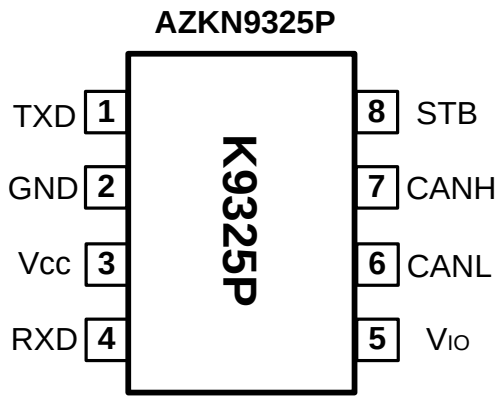
[3] See Figure 5.

[4] See Figure 10.

[5] See Figure 11.

[6] Not tested in production; guaranteed by design.

Pin Configuration



AZKN9325P : SOP8

Pin Function Description

Pin Number	Mnemonic	Function
1	TXD	Transmit data input; internally pulled up to V_{IO}
2	GND	Ground supply
3	V_{CC}	Supply voltage
4	RXD	Receive data output; reads out data from the bus lines
5	V_{IO}	Supply voltage for I/O level adapter
6	CANL	LOW-level CAN bus line
7	CANH	HIGH-level CAN bus line
8	STB	Standby mode control input; internally pulled up to V_{IO}

Detail Description of Part

The AZKN9325P is a high-speed CAN transceiver compliant with the signal improvement capability (SIC) specification of ISO 11898-2:2024. The V_{IO} supply pin should be connected to supply voltage of microcontroller (see Figure 6). The V_{IO} allows the supply range from 1.7 V to 5.5 V of the microcontroller to adjust the I/O signal levels of the TXD, RXD, and STB pins.

Operation Modes

The normal and standby are two operating modes for the AZKN9325P, which are selected by STB pin. The detail description of the operating modes related to both bus pins and RXD pin is listed in the Table 1.

- **Normal mode**

  When STB pin ties to logic LOW, the AZKN9325P will switch to the normal mode. In the normal mode, the driver will translate the logic state of TXD to differential output of HS CAN. The data rate of driver is up to the 8 Mbps with both the controlled slew rate and common mode voltage, which is Amazing's property. So that the driver performs the low common mode noise and has the low EME performance, which is evaluated by IEC 61967-4.

  The normal receiver with the ±12 V common mode range operates in the normal mode, which is also Amazing's property. The normal receiver translates the differential signal of HS CAN to the digital output of RXD with data rate up to 8 Mbps. The EM Immunity of normal receiver is evaluated by IEC 62132-4.

  The loop delay symmetry from TXD to RXD is optimized by both driver and normal receiver in the AZKN9325P.

- **Standby mode**

  When the voltage of pin V_{IO} rises above the undervoltage detection level $V_{uvd(VIO)}$ for $t_{startup}$, the AZKN9325P finishes the power-on-reset procedure and the transceiver enters the selected mode (decided by pin STB). When the STB ties to logic HIGH, the AZKN9325P will switch to the standby mode. In the standby mode, both the driver and normal receiver are turned off so that the bus pins are biased to GND to save V_{CC} power. Only the low power receiver operates to monitor the activity of the bus so as to inform the microcontroller if go to the normal mode or not. The low-power receiver is supplied from V_{IO} and can detect the bus activity even if V_{IO} is the only available supply.

  In standby mode, the wake-up filter on the output of the low-power receiver ensures that only bus dominant and bus recessive states that persist longer than $t_{fltr(wake)bus}$ are reflected on pin RXD after a wake-up pattern has been detected. Therefore, the data on RXD is not exact but is a wake-up signal to microcontroller.

  The bus pins of the AZKN9325P bias to GND via input resistor so that it is passive behavior in the standby mode.

- **Remote wake-up via the CAN bus**

  For avoiding spurious wake-up event, the AZKN9325P could be awake from standby mode only when a wake-up pattern defined by ISO 11898-2:2024 is detected on bus.

  This dedicated wake-up pattern consists of three states.

  - a dominant state > $t_{wake(busdom)}$ followed by
  - a recessive state > $t_{wake(busrec)}$ followed by
  - a dominant state > $t_{wake(busdom)}$

  Before a complete wake-up pattern is detected, dominant and recessive bits which are shorter than $t_{wake(busdom)}$ and $t_{wake(busrec)}$ respectively will be ignored and pin RXD will be kept logic high.

  This dominant-recessive-dominant pattern must be received within $t_{to(wake)bus}$ (see Figure 4). Otherwise, the internal wake-up logic will be reset. Therefore, the complete wake-up pattern must be resent again to trigger a valid wake-up event.

  After a complete wake-up pattern is detected, bus dominant or bus recessive states that persist longer than $t_{fltr(wake)bus}$ will be reflected on pin RXD. The AZKN9325P will remain in standby mode until microcontroller ties STB pin to logic LOW.

Fail-safe Protection

- **TXD dominant time-out function**

  The function of "TXD dominant time-out" prevents the failure of the hardware or software from keeping the bus in the dominant state. The failure causes the bus to be blocked all communication.

The timer of "TXD dominant time-out" is started when TXD pin is set to LOW. If the time of TXD pin in the LOW state is longer than $t_{to(dom)TXD}$, the driver will be turn off to release the bus. The timer of "TXD dominant time-out" will be reset when TXD pin is set to HIGH. Therefore, the minimum data rate of 25 kbps is defined by the function of "TXD dominant time-out".

- **Pull-up of TXD and STB input pins**
  The pins of both TXD and STB with internal pull-ups to V_{IO} are safe-guarantee design due to one or both of these pins in floating condition. When TXD pin is internally pulled up, the transmitter is forced into the recessive state. When STB pin is internally pulled up, the AZKN9325P is forced into the low power standby mode. By the way, the pull-up currents will be generated if the pins are biased to low state. In standby mode, both pins should be held HIGH to reduce the current.

- **Undervoltage detection on pins V_{CC} and V_{IO}**
  The undervoltage detection is the protection function to avoid the abnormal operation of V_{CC} and V_{IO} power.
  If V_{CC} drops below the V_{CC} undervoltage detection level $V_{uvd(VCC)}$ for $t_{det(uv)VCC}$, the transceiver enters standby mode. The logic state of STB and TXD pins are ignored until V_{CC} has recovered.
  If V_{IO} drops below the V_{IO} undervoltage detection level $V_{uvd(VIO)}$ for $t_{det(uv)VIO}$, the transceiver enters off mode. When the transceiver is in off mode, the logic state of STB and TXD pins are ignored and the transceiver will switch off and disengage from the bus (high Z) until V_{IO} has recovered.

- **Overtemperature protection**
  When the virtual junction temperature exceeds the shutdown junction temperature, $T_{J(sd)}$, the output of the drivers will be disabled to protect the AZKN9325P from burn out issue. In this state, both CANH and CANL are biased to the recessive level no matter what the logic level of TXD pin is and the receiver still remains operational. When the temperature falls below $T_{J(sd)}$, the overtemperature protection will be released. The typical $T_{J(sd)}$ is designed as 190 °C under V_{CC} = 5.0 V.

- **I/O levels**
  The signal levels on pins TXD, RXD and STB could be adjusted to the I/O levels of the microcontroller by connecting pin V_{IO} on the AZKN9325P to the microcontroller supply voltage. Moreover, pin V_{IO} provides the supply voltage for the circuits operating in standby mode, this makes the standby mode function work normally while there is no supply voltage on pin V_{CC}.
  Pin STB on the AZKN9325P is capable of filtering out spurious transitions from the microcontroller with a filter time of $t_{fltr(STB)}$.

High-Immunity Communication

- **High EFT coupling Immunity**
  The AZKN9325P has high EFT coupling immunity on the bus line under the normal operation. The output of transmitter (CANH and CANL) and the output of receiver (RXD) could be recovered after next bit when the high voltage the pulse of EFT coupled to the bus line through the coupling box (CCC method), as Figure 8. So the AZKN9325P has more ability to communicate with low Bit-Error-Rate (BER) under the high noise environment.

High Protection for All Pins

- **±8 kV System-level ESD for CANH and CANL**
  The AZKN9325P is embedded high voltage ±42 V TVS on the pins of CANH and CANL to achieve IEC 61000-4-2 contact ±8 kV of the system-level ESD protection. In the evaluation of system-level ESD, both CANH and CANL of the AZKN9325P are zapped by ESD gun referred to GND on the evaluation board.

- **HBM ±5 kV, MM ±400 V and CDM ±800 V for all pins**
  To achieve the high reliability and high assembly yield rate, the AZKN9325P have high ESD specification of the component-level for both HBM and MM. With the high robust whole-chip ESD protection, the AZKN9325P can still sustain no matter the ESD pulse comes from power pin or the I/O pins. For the IC self-discharge issue, the CDM protection level of the AZKN9325P is up to ±800 V.

Mode	Normal	Standby	Off[1]
Pin STB	LOW	HIGH	X
Driver	Enabled	Disabled (biased to GND)	High Z
Receiver	HS RX enabled	LP RX enabled	All RX disabled
Pin RXD	Follows bus state	High if no wake-up pattern detected[2]	High Z
		Follows bus state if wake-up pattern detected[2]	

[1] Off mode is entered when the voltage on pin V_{IO} is below undervoltage detection level $V_{uvd(VIO)}$.

[2] See Figure 4.

Table 1. Operating modes

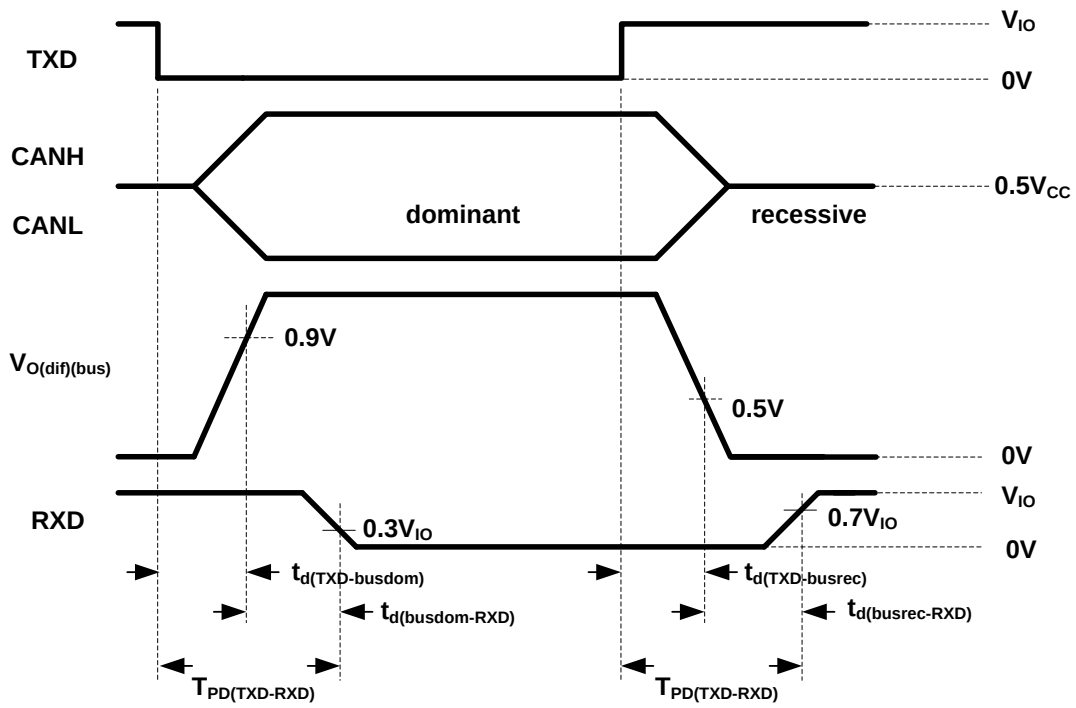


Figure 1. Timing diagram of the CAN transceiver

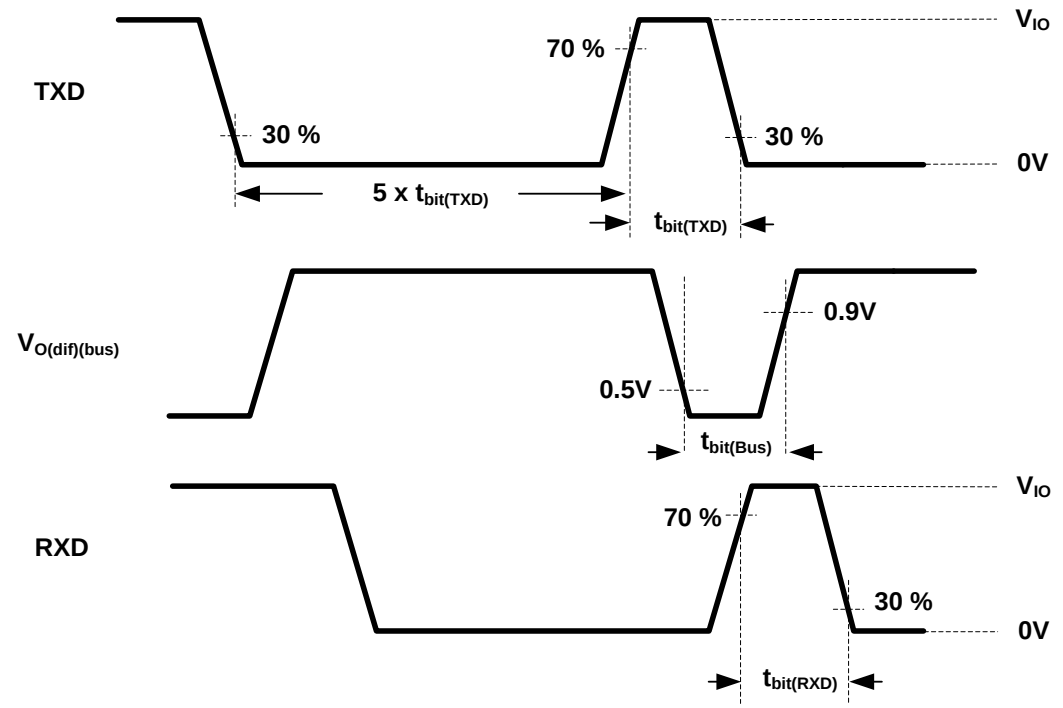


Figure 2. Timing diagram for loop delay symmetry

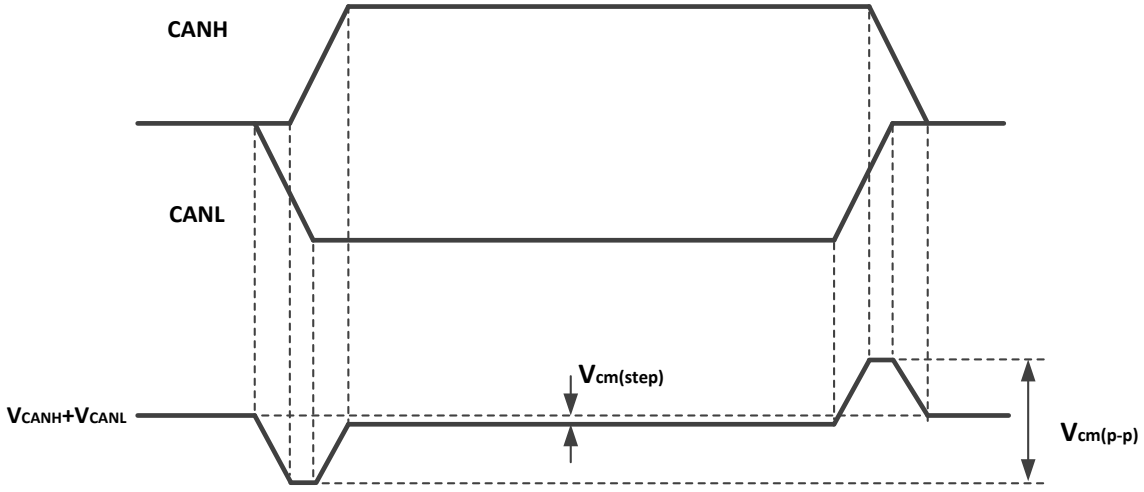


Figure 3. CAN bus common-mode voltage

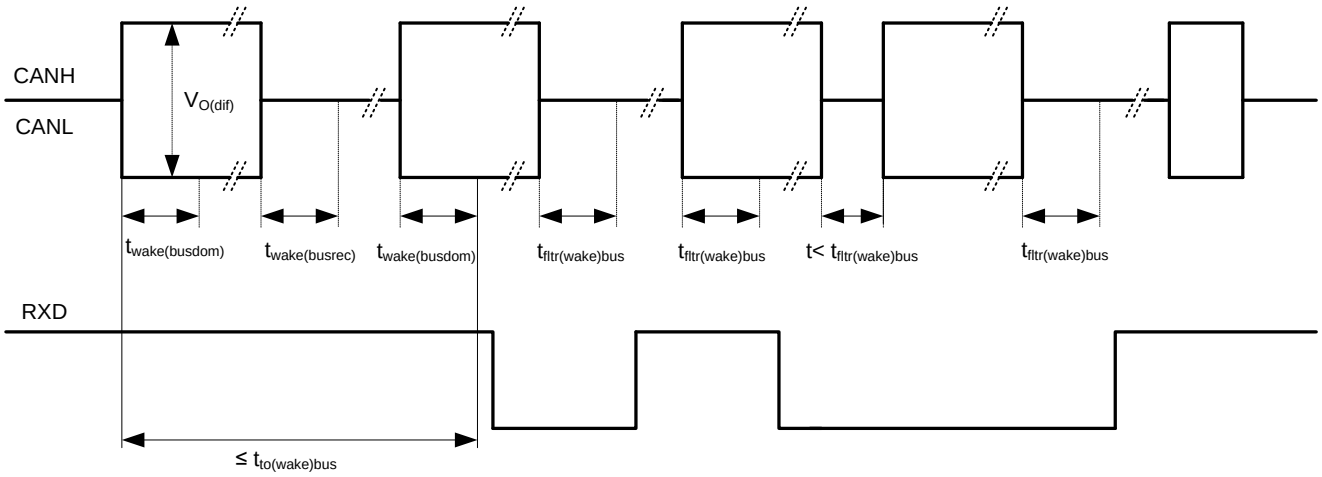


Figure 4. Timing diagram for wake-up pattern

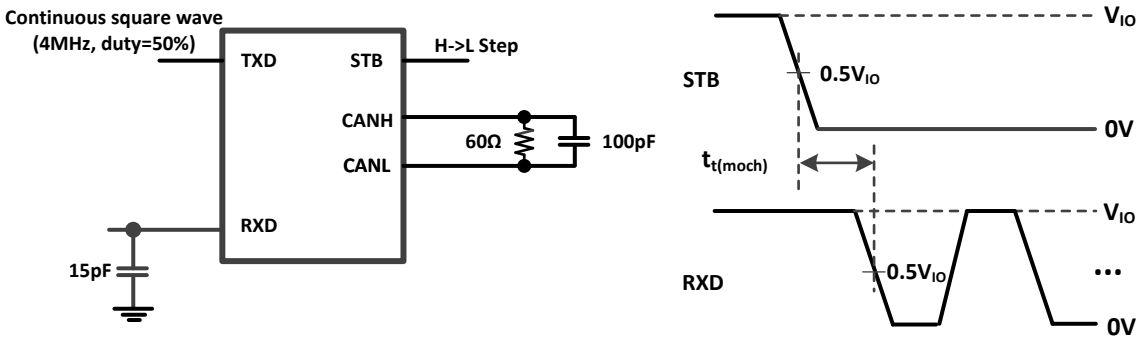


Figure 5. Timing diagram and test circuit for mode change transition time

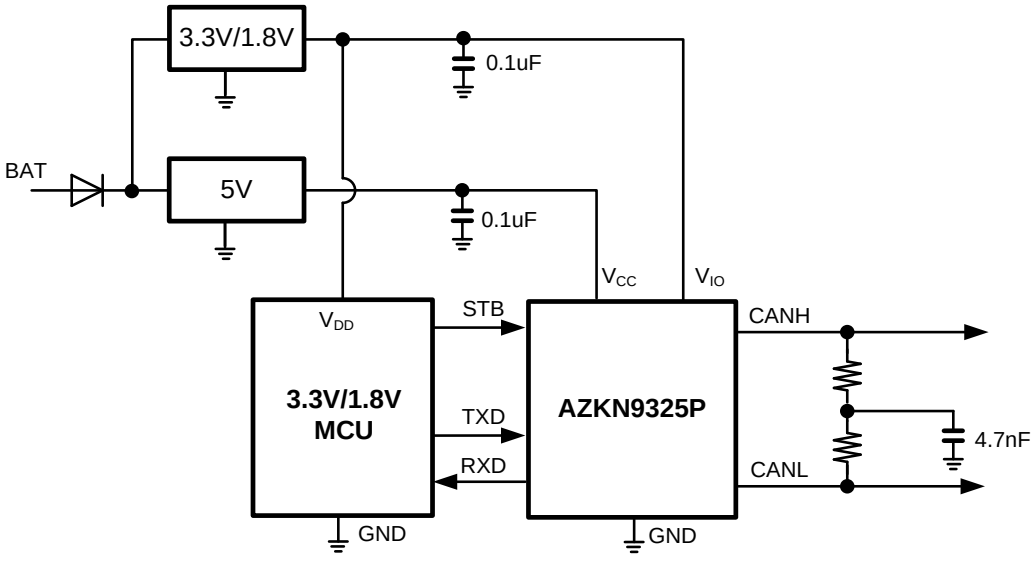


Figure 6. Typical application circuit for AZKN9325P with 3.3V or 1.8V MCU

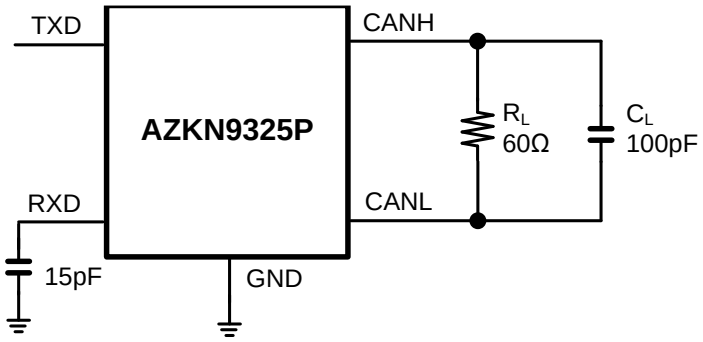


Figure 7. CAN transceiver timing test circuit

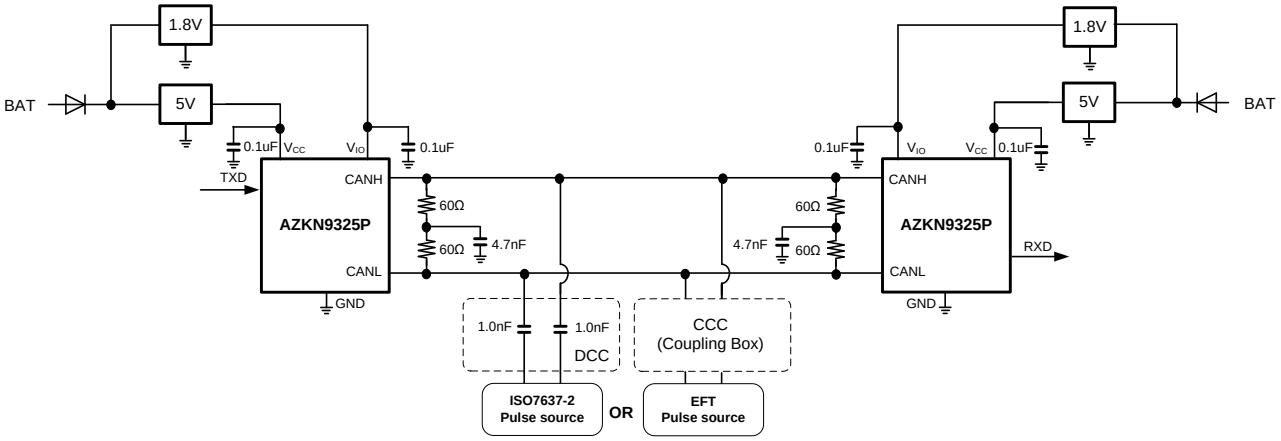


Figure 8. ISO7637-2 and EFT coupling test circuit for AZKN9325P

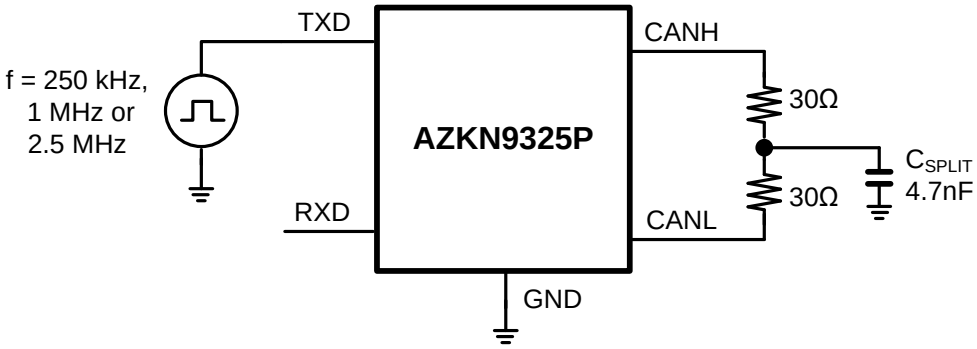


Figure 9. Test circuit for measuring transmitter driver symmetry

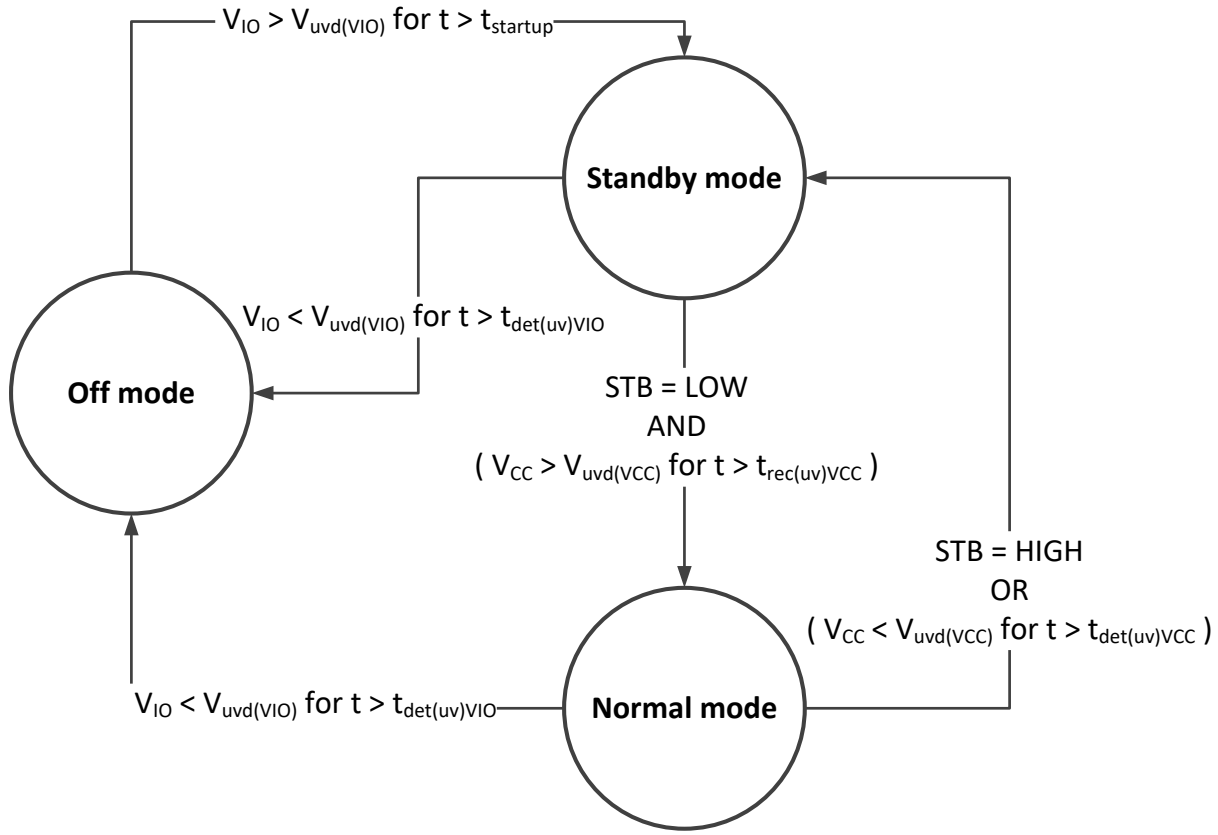


Figure 10. AZKN9325P state diagram

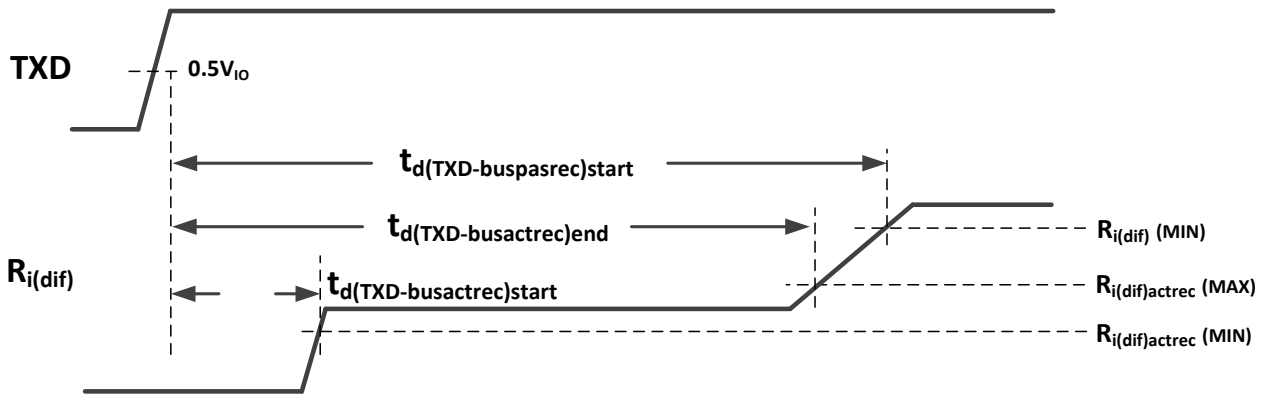
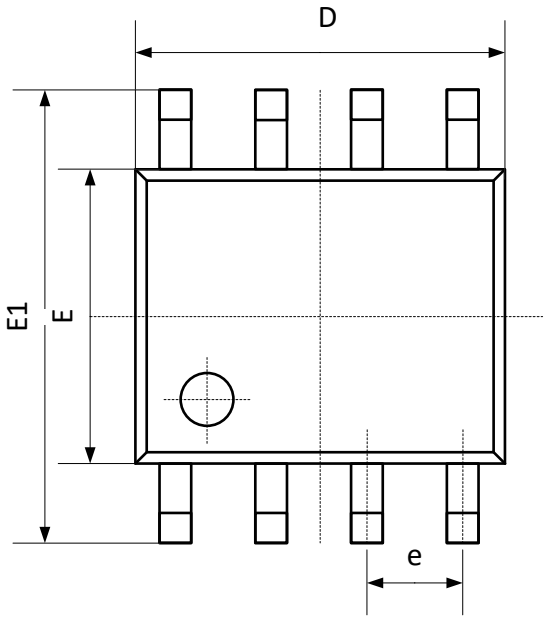


Figure 11. Timing diagram of transmitter input resistance for dominant-to-recessive transition according to ISO11898-2:2024 parameter set C

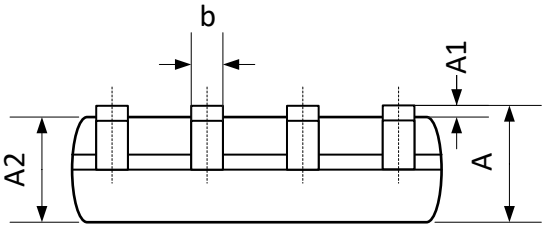
Mechanical Details

PACKAGE DIAGRAMS

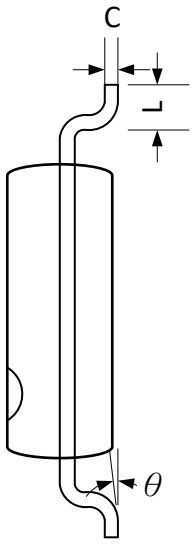
TOP VIEW



SIDE VIEW



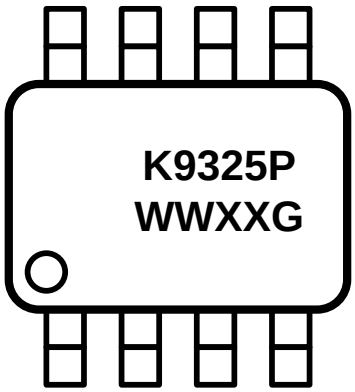
END VIEW



PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	min	Max	min	max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.55	0.049	0.061
b	0.33	0.51	0.013	0.020
C	0.17	0.26	0.007	0.010
D	4.70	5.10	0.185	0.201
E	3.70	4.10	0.146	0.161
E1	5.80	6.20	0.228	0.244
e	1.27 BSC		0.05BSC	
L	0.40	1.27	0.016	0.050
θ	0	8	0	8

MARKING CODE



K9325P = Device Code

WW = Date Code ; XX = Control Code

G = Green Part Indication

Part Number	Marking Code
AZKN9325P.RDG	K9325P WWXXG

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZKN9325P.RDG	Green	T/R	13 inch	2,500/reel	1 reel = 2,500/box	5 boxes =12,500/carton

Revision History

Revision Date	Modification Description
2026/3/2	Formal Release