AZKN9135P

±42V Fault Protected High-Speed CAN Transceiver with IEC 61000-4-2 contact ±8kV ESD Protection

Features

- ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 compliant for 2Mbps and 5Mbps CAN FD
- Fault voltage up to ±42 V for bus pins
- Integrated ESD and Surge Transient Voltage Suppressor (TVS) for bus pins
- TVS protection Immunities for bus terminals
  ±8kV IEC 61000-4-2, Contact Discharge
  ±10kV IEC 61000-4-2, Air Discharge
  ±80V IEC 61000-4-5, Surge (8/20 μs, 2 Ω)
- HBM ±5k V ESD protection for all pins
- HBM ±8kV ESD protection for bus pins
- MM ±400 V ESD protection for all pins
- High CDM protection up to ±800 V for all pins
- Latch up immunity up to ±400 mA for all pins
- High IEC 61000-4-4 Electrical Fast Transient (EFT) coupling immunity for bus pins under communication
- Capability to withstand ISO7637-2 standard pulses 1, 2a, 3a, and 3b
- Capability for both low ElectroMagnetic Emission (EME) and high ElectroMagnetic Immunity (EMI)
- Wide range digital inputs allow for direct interfacing with 3.3V to 5.0V microcontrollers, provided the microcontroller I/Os are 5V tolerant
- Ideal passive behavior to CAN bus with supply power off
- Transmit Data (TXD) dominant time-out function
- Undervoltage detection on the pins of V_{CC} power
- Current-limitation and thermal shutdown for the driver design
- AEC-Q100 qualified

Applications

- Automotive Electronics
- Industrial Control and Instrumentation Networks
- Motor Control
- Battery Control

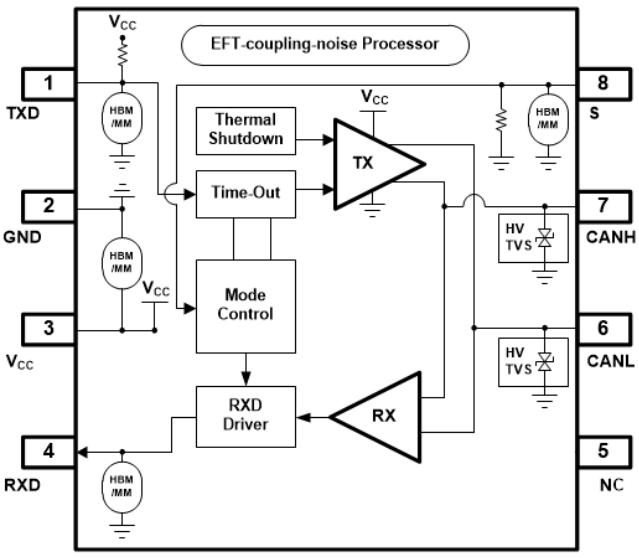
Description

AZKN9135P is a ±8 kV IEC 61000-4-2 protected Controller Area Network (CAN) transceiver IC. It serves as an interface between a CAN protocol controller (MCU) and the physical two-wire CAN bus. This device operates at 5 V power supply and is fully compliant with ISO 11898-2:2016 standard for CAN FD application. The data rate of both driver and receiver is up to 5Mbps to support the high-speed application of the CAN FD.

AZKN9135P has the capabilities of both the ±40 V common mode range of the receiver and the low EME of the transmitter, which has been patented as the Amazing's intellectual property. Moreover, the whole-chip design of the AZKN9135P can sustain high EFT coupling under communication.

AZKN9135P is a robust CAN transceiver, which features ±42 V fault protection to sustain the DC short voltage on the bus pins. Moreover, AZKN9135P has ±80 V surge protection immunity to avoid the possible damage from the EOS events. In addition, the whole-chip ESD protection immunity of AZKN9135P can sustain HBM ±5 kV, MM ±400 V and CDM ±800 V, which is satisfied with the AEC Q100 specifications to overcome the ESD zapping under the worst manufacture environment.

Functional Block of AZKN9135P



Thermal Characteristics

PARAMETER	SYMBOL	Conditions	Value	UNIT
Thermal resistance from virtual junction to ambient	θ_{JA} [1]	P_H = 70 mW under the air flow rate = 0 (m/s) in the ambient temperature [2]	90.97	°C/W

[1] The thermal resistance between virtual junction and ambient is $\theta_{JA}= (T_J - T_{AMB})/P_H$, where T_J is the virtual junction temperature and T_{AMB} is the ambient temperature under the power dissipation of PH.

[2] According to JEDEC JESD51-2 and JESD51-7 at natural convection on 2s2p board with two inner copper layers (Power/Ground thickness: 35 um; Signal thickness: 70 um).

Absolute Maximum Ratings [1]

PARAMETER	SYMBOL	MIN	MAX	UNIT
DC voltage on CANH, CANL	V_{CANH},V_{CANL}	-42	42	V
DC voltage between pin CANH and pin CANL	$V_{(CANH-CANL)}$	-50	50	V
DC voltage on all other pins	V_X	-0.3	7	V
Transient voltage on pins CANH and CANL For ISO 7637-2 pulse 1 [2]	V_{trt1}	-100	-	V
Transient voltage on pins CANH and CANL For ISO 7637-2 pulse 2a [2]	V_{trt2a}	-	75	
Transient voltage on pins CANH and CANL For ISO 7637-2 pulse 3a [2]	V_{trt3a}	-150	-	V
Transient voltage on pins CANH and CANL For ISO 7637-2 pulse 3b [2]	V_{trt3b}	-	100	V
System-level ESD (IEC 61000-4-2, Contact Discharge) -- at pins CANH, CANL	$V_{ESD(contact)}$	-8	8	kV
System-level ESD (IEC 61000-4-2, Air-Gap Discharge) -- at pins CANH, CANL	$V_{ESD(air)}$	-10	10	kV
Surge (IEC 61000-4-5) at pins CANH, CANL [3]	V_{SURGE}	-80	80	V
HBM ESD (Human Body Model; 100pF; 1.5 kΩ) -- at any pins [4]	V_{HBM}	-5	5	kV
HBM ESD (Human Body Model; 100pF; 1.5 kΩ) -- at pins CANH, CANL [4]	V_{HBM}	-8	8	kV
MM ESD (Machine Model; 200pF) -- at any pins [5]	V_{MM}	-400	400	V
CDM ESD (Charged Device Model; field induced charge) -- at any pins [6]	V_{CDM}	-800	800	V
Virtual junction temperature	T_J	-40	150	°C
Storage temperature	T_{STO}	-55	150	°C

[1] Stresses listed above may cause permanent damage to the device under “Maximum Ratings”. This is a stress rating only and functional operation of the device at those or other conditions above those indicated in the operational listings of this specification are not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

[2] Verified by thirty-party to ensure both CANH and CANL can withstand ISO 7637-2 automotive transient test pulses 1, 2a, 3a and 3b. The DUT is evaluated by the DCC method with coupling capacitance of 1nF connected between the pulse source and the cable of CANH and CANL respectively, which is shown in Figure 4.

[3] Applied surge source voltage: tp =8/20 μs, 2 Ω source impedance.

[4] Verified by thirty-party referred to AEC Q100-002

[5] Verified by thirty-party referred to AEC Q100-003

[6] Verified by thirty-party referred to AEC Q100-011

DC Electrical Characteristics

(V_{CC} = 4.75 V to 5.25 V; T_{AMB} = -40 °C to +125 °C; R_L = 60 Ω unless otherwise noted. Typical values are at V_{CC} = 5 V and T_{AMB} = 25 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Internal Supply : V_{CC}						
Supply voltage	V_{CC}		4.75	-	5.25	V
Undervoltage detection voltage on pin V_{CC}	$V_{uvd(VCC)}$		3.5	4.0	4.5	V
Supply current	I_{CC}	Silent mode				
		V_S=V_{CC}	0.1	1.5	2.5	mA
		Normal Mode				
		Recessive; V_{TXD}=V_{CC}	2.5	5	12	mA
		Dominant; V_{TXD}=0 V	20	40	70	mA
		Dominant; V_{TXD}=0 V; Short circuit on bus lines; -3 V < (V_{CANH} = V_{CANL}) < +18 V	2.5	90	120	mA
Bus lines : CANH and CANL						
Dominant output voltage	$V_{O(dom)}$	Normal Mode; V_{TXD}= 0 V; $t < t_{to(dom)TXD}$				
		pin CANH; R_L = 50 Ω to 65 Ω	2.75	3.5	4.5	V
		pin CANL; R_L = 50 Ω to 65 Ω	0.5	1.5	2.25	V
Transmitter dominant voltage symmetry	$V_{dom(TX)sym}$	$V_{dom(TX)sym}$ = V_{CC}-V_{CANH}-V_{CANL}	-400	-	+400	mV
Transmitter voltage symmetry	V_{TXsym}	V_{TXsym}=V_{CANH}+V_{CANL}; [2] f_{TXD}=250KHz, 1MHz and 2.5MHz; [3] C_{SPLIT}=4.7nF	0.9V_{CC}	-	1.1V_{CC}	
Bus differential output voltage	$V_{O(dif)bus}$	Normal Mode; V_{TXD}=0 V; $t < t_{to(dom)TXD}$				
		R_L = 50 Ω to 65 Ω	1.5	-	3	V
		R_L = 45 Ω to 70 Ω	1.4	-	3.3	V
		R_L = 2240 Ω	1.5	-	5	V
		recessive; no load				
		Normal mode; V_{TXD} = V_{CC}	-50	-	+50	mV
Recessive output voltage	$V_{O(rec)}$	Normal/Silent mode; V_{TXD} = V_{CC}; no load	2	0.5V_{CC}	3	V
Differential receiver threshold voltage	$V_{th(RX)dif}$	Normal/Silent mode; $V_{CM(CAN)}$ = -40 V to +40 V [1]	0.5	0.7	0.9	V
Receiver recessive voltage	$V_{rec(RX)}$	Normal/Silent mode; $V_{CM(CAN)}$ = -40 V to +40 V [1]	-4	-	0.5	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Receiver dominant voltage	$V_{dom(RX)}$	Normal/Silent mode; $V_{CM(CAN)}$ = -40 V to +40 V [1]	0.9	-	9.0	V
Differential receiver hysteresis voltage	$V_{hys(RX)dif}$	Normal/Silent mode; $V_{CM(CAN)}$ = -40 V to +40 V [1]		100		mV
Dominant short-circuit output current	$I_{O(SC)dom}$	Normal Mode; V_{TXD} = 0V; $t < t_{to(dom)TXD}$;V_{CC} = 5V				
		Pin CANH; V_{CANH} = -15 V to 40 V	-115	-70		mA
		Pin CANL; V_{CANL} = -15 V to 40 V		65	115	mA
Recessive short-circuit output current	$I_{O(SC)rec}$	Normal mode; $V_{TXD} = V_{CC}$ V_{CANH}=V_{CANL}= -27 V to +32 V	-5	-	+5	mA
Leakage current	I_L	V_{CC} = 0 V or V_{CC} = shorted to ground via 47 kΩ; $V_{CANH} = V_{CANL}$ = 5 V	-5	-	+5	μA
Input resistance	R_i	-2 V≦V_{CANH}≦+7 V; -2 V≦V_{CANL}≦+7 V	9	15	28	kΩ
Input resistance deviation	ΔR_i	0 V≦V_{CANH}≦+5 V; 0 V≦V_{CANL}≦+5 V [2]	-1	-	+1	%
Differential input resistance	$R_{i(dif)}$	-2 V≦V_{CANH}≦+7 V; -2 V≦ V_{CANL}≦+7 V	19	30	52	kΩ
Common-mode input capacitance	$C_{i(cm)}$	[2]	-	-	20	pF
Differential input capacitance	$C_{i(dif)}$	[2]	-	-	10	pF
Mode control input : S						
High-level input voltage	V_{IH}		2	-	Vcc+0.3	V
Low-level input voltage	V_{IL}		-0.3Vcc	-	+0.8	V
High-level input current	I_{IH}	$V_S = V_{CC}$	1	7	15	μA
Low-level input current	I_{IL}	V_S = 0 V	-1	0	+1	μA
Transmit data input : TXD						
High-level input voltage	V_{IH}		2	-	V_{CC}+0.3	V
Low-level input voltage	V_{IL}		-0.3	-	+0.8	V
High-level input current	I_{IH}	$V_{TXD} = V_{CC}$	-5	-	+5	μA
Low-level input current	I_{IL}	V_{TXD} = 0 V	-280	-170	-30	μA
Input capacitance	C_i	[2]	-	5	10	pF
Receive data output : RXD						
High-level output current	I_{OH}	$V_{RXD} = V_{CC}$ - 0.4 V	-13	-8	-2	mA
Low-level output current	I_{OL}	V_{RXD} = 0.4 V; bus dominant	2	7	15	mA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Temperature Protection						
Shutdown temperature	$T_{J(sd)}$	[2]	-	190	-	°C

[1] $V_{CM(CAN)}$ is the common mode voltage of CANH and CANL.

[2] Not tested in production; guaranteed by design.

[3] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Figure 6.

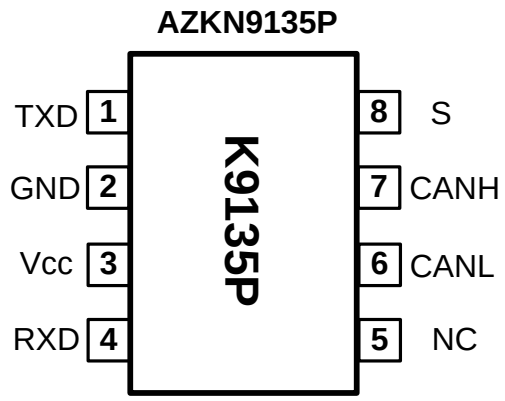
Switching Characteristics

(V_{CC} = 4.75 V to 5.25 V; T_{AMB} = -40 °C to +125 °C; R_L = 60 Ω unless otherwise noted. Typical values are at V_{CC} = 5 V and T_{AMB} = 25 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Transceiver timing; pins CANH, CANL, TXD and RXD; see Figure 1 and Figure 5						
Delay time from TXD to bus dominant	$t_{d(TXD-busdom)}$	Normal mode	-	40	-	ns
Delay time from TXD to bus recessive	$t_{d(TXD-busrec)}$	Normal mode	-	55	-	ns
Delay time from bus dominant to RXD	$t_{d(busdom-RXD)}$	Normal mode	-	65	-	ns
Delay time from bus recessive to RXD	$t_{d(busrec-RXD)}$	Normal mode	-	85	-	ns
Propagation delay from TXD to RXD	$t_{PD(TXD-RXD)}$	Normal mode	50	-	230	ns
Bit time on Bus	$t_{bit(Bus)}$	$t_{bit(TXD)}$ = 500 ns [1]	435	-	530	ns
		$t_{bit(TXD)}$ = 200 ns [1]	155		210	ns
Bit time on pin RXD	$t_{bit(RXD)}$	$t_{bit(TXD)}$ = 500 ns [1]	400	-	550	ns
		$t_{bit(TXD)}$ = 200 ns [1]	120		220	ns
Receiver timing symmetry	Δt_{Rec}	$\Delta t_{Rec} = t_{bit(RXD)} - t_{bit(Bus)}$				
		$t_{bit(TXD)}$ = 500 ns	-65	-	+40	ns
		$t_{bit(TXD)}$ = 200 ns	-45	-	+15	ns
TXD dominant time-out time	$t_{to(dom)TXD}$	V_{TXD} = 0 V; Normal mode	0.8	3	8	ms

[1] See Figure 2.

Pin Configuration



AZKN9135P : SOP8

Pin Function Description

Pin Number	Mnemonic	Function
1	TXD	Transmit data input
2	GND	Ground supply
3	V_{CC}	Supply voltage
4	RXD	Receive data output; reads out data from the bus lines
5	NC	Not connected
6	CANL	LOW-level CAN bus line
7	CANH	HIGH-level CAN bus line
8	S	Silent mode control input

Detail Description of Part

AZKN9135P is a high-speed CAN transceiver compliant with the ISO 11898-2:2016. This part has a silent node to switch off transmitter for saving power. AZKN9135P also includes TXD dominant time-out function, pull-up of input pins, undervoltage detection and overtemperature protection for fail-safe protection.

Operation Modes

The normal and silent are two operating modes for AZKN9135P, which are selected by S pin. The detail description of the operating modes related to both bus pins and RXD pin is listed in the Table 1.

- **Normal mode**

  When S pin ties to logic LOW, AZKN9135P will switch to the normal mode. In the normal mode, the driver will translate the logic state of TXD to differential output of HS CAN. The data rate of driver is up to the 5Mbps with both the controlled slew rate and common mode voltage, which is Amazing's property. So that the driver performs the low common mode noise and has the low EME performance, which is evaluated by IEC 61967-4.

  The normal receiver with the ±40 V common mode range operates in the normal mode, which is also Amazing's property. The normal receiver translates the differential signal of HS CAN to the digital output of RXD with data rate up to 5Mbps. The EM Immunity of normal receiver is evaluated by IEC 62132-4.

  The loop delay symmetry from TXD to RXD is optimized by both driver and normal receiver in AZKN9135P.

- **Silent mode**

  When the S ties to logic HIGH, AZKN9135P will switch to the silent mode. In the silent mode, the transmitter is turned off. Only the receiver operates normally.

Fail-safe Protection

- **TXD dominant time-out function**

  The function of "TXD dominant time-out" prevents the failure of the hardware or software from keeping the bus in the dominate state. The failure causes the bus to be blocked all communication. The timer of "TXD dominate time-out" is started when TXD pin is set to LOW. If the time of TXD pin in the LOW state is longer than $t_{to(dom)TXD}$, the driver will be turn off to release the bus. The timer of "TXD dominate time-out" will be reset when TXD pin is set to HIGH. Therefore, the minimum data rate of 25kbps is defined by the function of "TXD dominant time-out".

- **Internal biasing of TXD and S input pins**

  The pin of TXD has an internal pull-up to VCC and the pin of S has an internal pull-down to GND. These are safe-guarantee design due to one of these pins in floating condition. When TXD pin is internally pulled up, the transmitter is forced into the recessive state. When S pin is internally pulled down, AZKN9135P is forced into the normal mode. By the way, the pull-up or pull-down currents will be generated if the pins are biased to the opposite direction of the internal biasing.

- **Undervoltage detection on pins V_{CC}**

  When V_{CC} drops below the V_{CC} undervoltage detection level, $V_{uvd(VCC)}$, the transceiver will switch to off mode. The logic state of S and TXD pins will be ignored and the transceiver will switch off and disengage from the bus (zero load) until V_{CC} has been recovered. The undervoltage detection is the protection function to avoid the abnormal operation of V_{CC} power.

- **Overtemperature protection**

  When the virtual junction temperature exceeds the shutdown junction temperature, $T_{J(sd)}$, the output of the drivers will be disabled to protect AZKN9135P from burn out issue. In this state, both CANH and CANL are biased to the recessive level no matter what the logic level of TXD pin is and the receiver still remains operational. When the temperature falls below $T_{J(sd)}$, the overtemperature protection will be released. The typical $T_{J(sd)}$ is designed as 190°C under V_{CC} = 5.0 V.

High-Immunity Communication

- **High EFT coupling Immunity**
  AZKN9135P has high EFT coupling immunity on the bus line under the normal operation. The output of transmitter (CANH and CANL) and the output of receiver (RXD) could be recovered after next bit when the high voltage the pulse of EFT coupled to the bus line through the coupling box (CCC method), as Figure 4. So the AZKN9135P has more ability to communicate with low Bit-Error-Rate (BER) under the high noise environment.

High Protection for All Pins

- **±8 kV System-level ESD for CANH and CANL**
  AZKN9135P is embedded high voltage ±42 V TVS on the pins of CANH and CANL to achieve IEC 61000-4-2 contact ±8 kV of the system-level ESD protection. In the evaluation of system-level ESD, both CANH and CANL of AZKN9135P are zapped by ESD gun referred to GND on the evaluation board.

- **Basic surge protection for CANH and CANL**
  AZKN9135P pass ±80V of the IEC 61000-4-5 (8/20μs) with 2Ω of source impedance for directly injection. With both the surge and fault protection, AZKN9135P can efficiently prevent the EOS event in the harsh environment.

- **HBM 5kV, MM 400V and CDM 800V for all pins**
  To achieve the high reliability and high assembly yield rate, AZKN9135P have high ESD specification of the component-level for both HBM and MM. With the high robust whole-chip ESD protection, AZKN9135P can still sustain no matter the ESD pulse comes from power pin or the I/O pins. For the IC self-discharge issue, the CDM protection level of AZKN9135P is up to ±800 V.

Table 1. **Operating modes**

S Pin		Low	High
Mode		Normal	Silent
Bus pins (CANH, CANL)		Dominant / Recessive	Recessive [1]
RXD	High	Recessive	Recessive
	Low	Dominant	Dominant

[1] In Silent mode, the receiver is active to receive BUS signals.

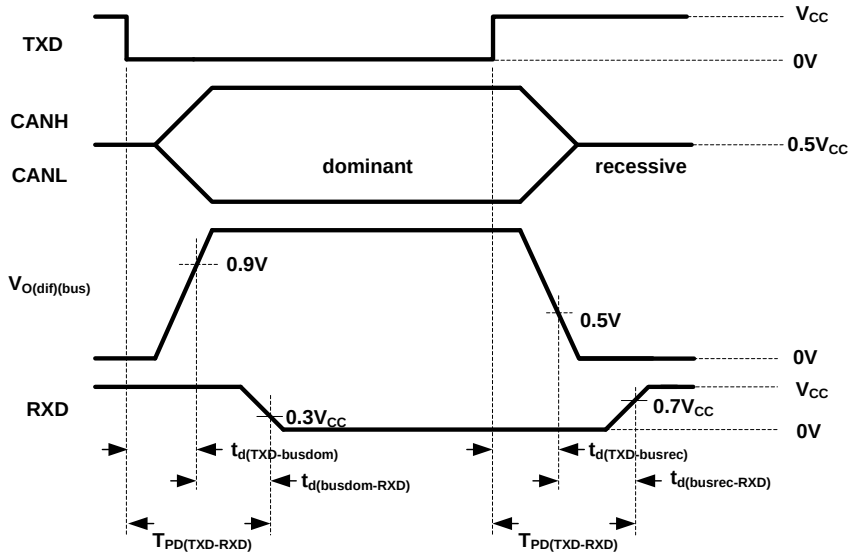


Figure 1. Timing diagram of the CAN transceiver.

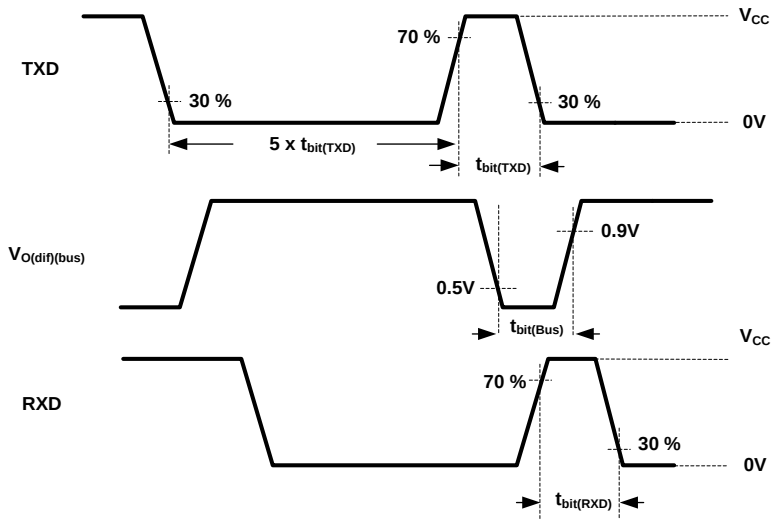


Figure 2. Timing diagram for loop delay symmetry.

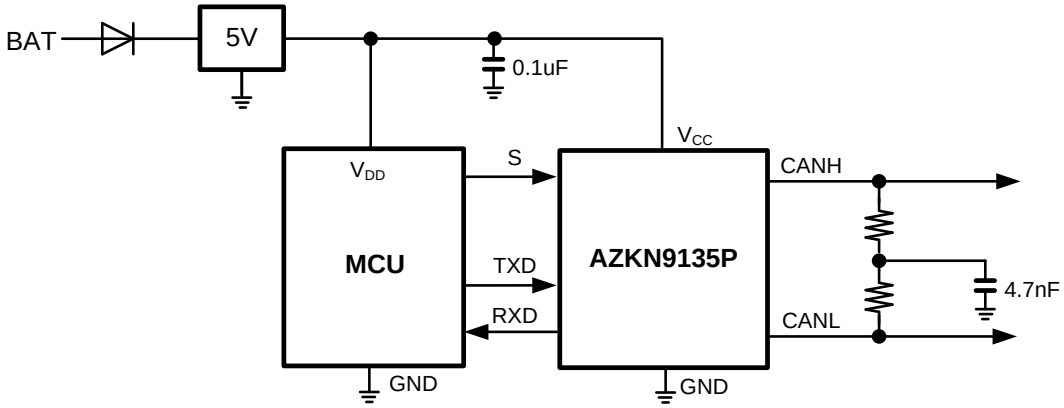


Figure 3. Typical application circuit for AZKN9135P with 5V MCU.

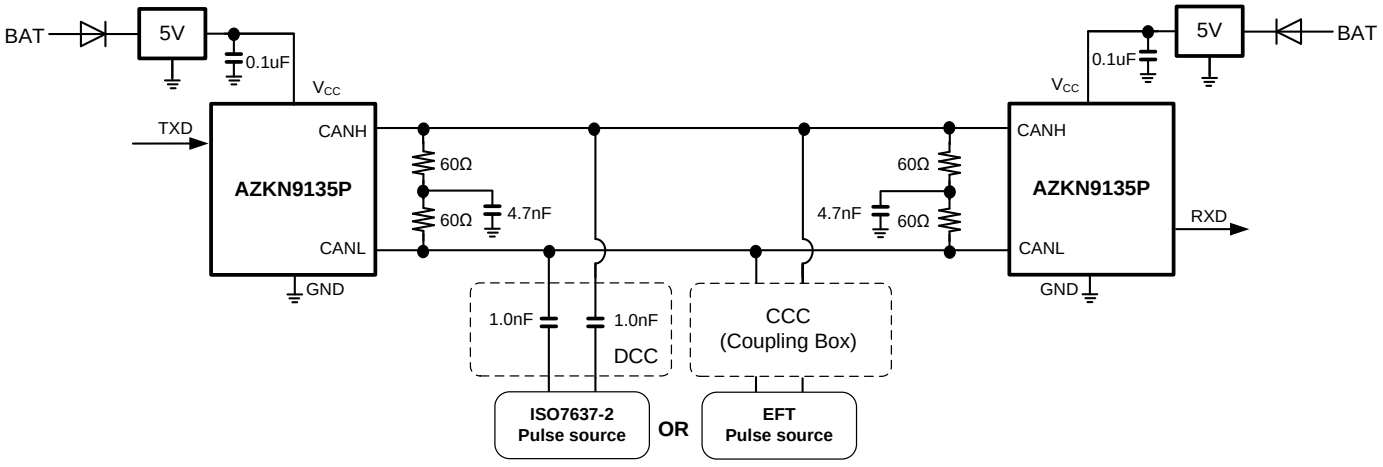


Figure 4. ISO 7637-2 DCC or EFT coupling test circuit for AZKN9135P.

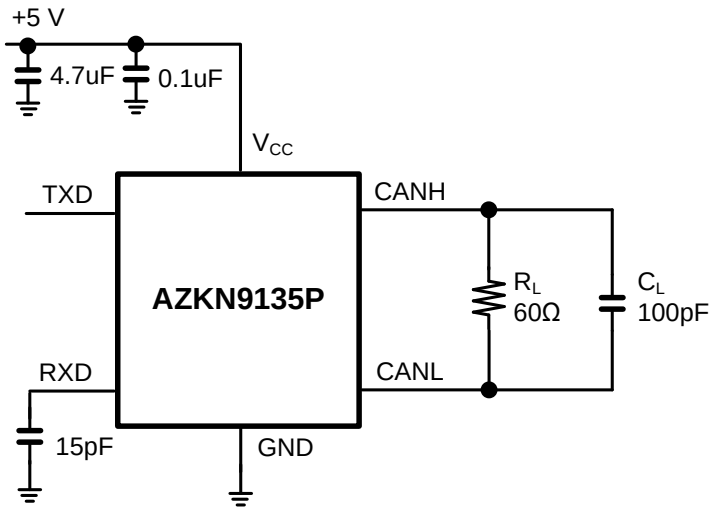


Figure 5. CAN transceiver timing test circuit.

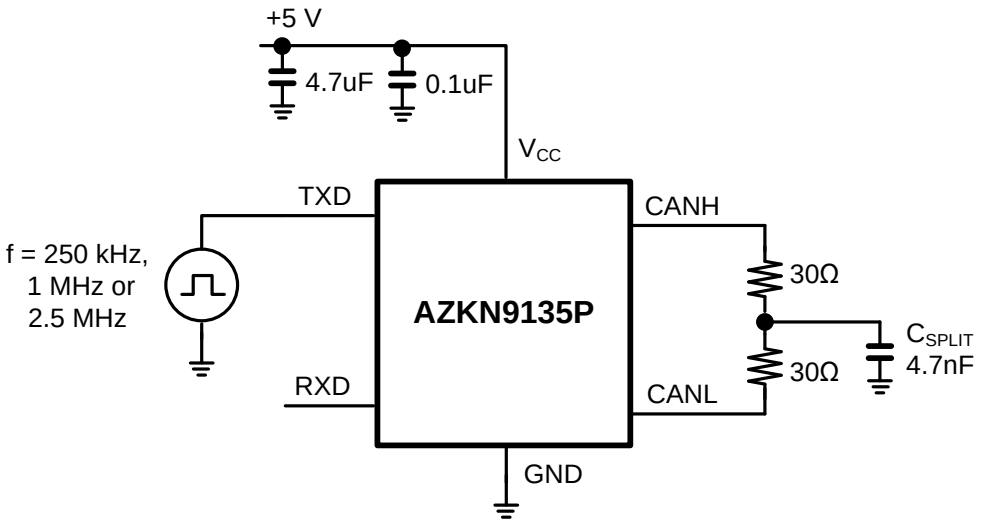
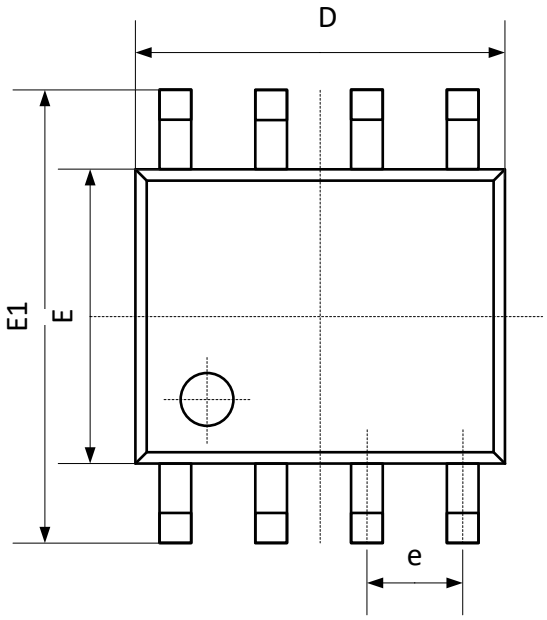


Figure 6. Test circuit for measuring transmitter driver symmetry.

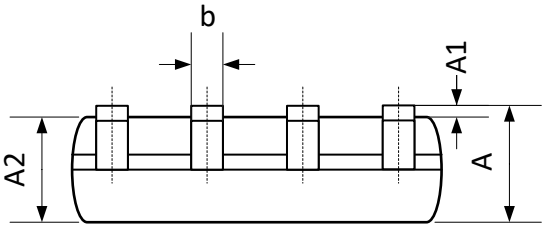
Mechanical Details

PACKAGE DIAGRAMS

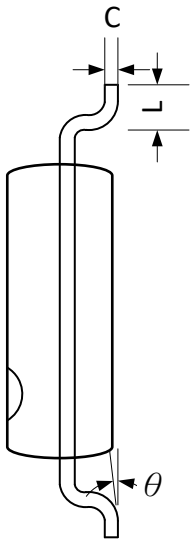
TOP VIEW



SIDE VIEW



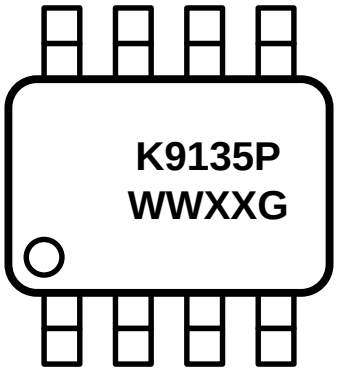
END VIEW



PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	min	Max	min	max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.55	0.049	0.061
b	0.33	0.51	0.013	0.020
C	0.17	0.26	0.007	0.010
D	4.70	5.10	0.185	0.201
E	3.70	4.10	0.146	0.161
E1	5.80	6.20	0.228	0.244
e	1.27 BSC		0.05BSC	
L	0.40	1.27	0.016	0.050
Θ	0	8	0	8

MARKING CODE



K9135P = Device Code

WW = Date Code ; XX = Control Code

G = Green Part Indication

Part Number	Marking Code
AZKN9135P.RDG	K9135P WWXXG

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZKN9135P.RDG	Green	T/R	13 inch	2,500/reel	1 reel=2,500/box	5 boxes =12,500/carton

Revision History

Revision Date	Modification Description
2023/10/6	Formal Release.
2023/10/30	Modify Function Block Diagram of AZKN9135P.