

Features

- ESD protect for 2 high-speed I/O channels
- Provide transient protection for each line to
IEC 61000-4-2 (ESD) $\pm 17\text{kV}$ (air/contact)
IEC 61000-4-5 (Lightning) 6.5A (8/20 μs)
- Low capacitance : 2.0pF typical
- Fast turn-on and low clamping voltage
- Array of ESD rated diodes with internal equivalent TVS (Transient Voltage Suppression) diode
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green part**
- **AEC-Q101 qualified**

Applications

- LVDS interface
- Video graphics cards
- USB2.0 power and data lines protection
- Monitors and flat panel displays
- Automotive application

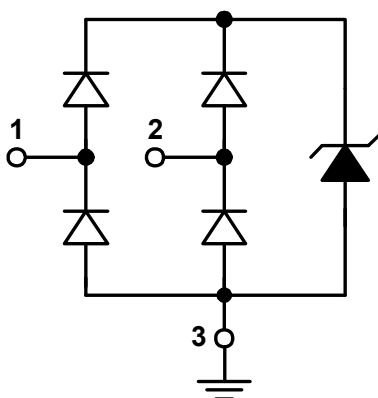
AZ9C39-02S is a high performance design which includes surge rated diode arrays to protect high speed data interfaces. The AZ9C39-02S has been specifically designed to protect sensitive components, which are connected to data and transmission lines, from over-voltage caused by Electrostatic Discharging (ESD), and Lightning.

AZ9C39-02S is a unique design which includes surge rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the internal ESD line or to the ground line. The internal unique design of clamping cell prevents over-voltage on the internal ESD line and on the I/O line, which is protecting any downstream components.

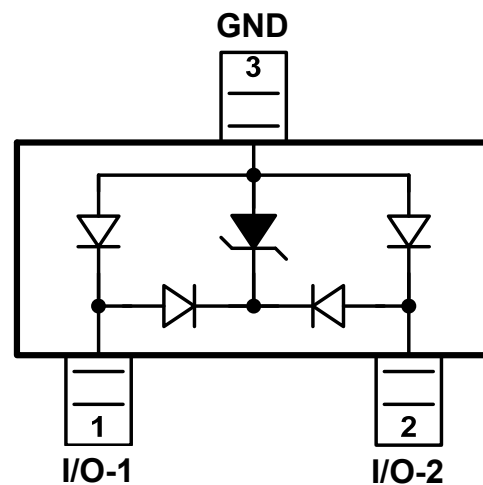
AZ9C39-02S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Description

Circuit Diagram



Pin Configuration



JEDEC SOT23-3L (Top View)



Specifications

Absolute Maximum Ratings			
Parameter	Symbol	Rating	Unit
Peak Pulse Current ($t_p = 8/20\mu s$)	I_{PP}	6.5	A
Operating Voltage	V_{DC}	5.5	V
ESD per IEC 61000-4-2 (Air)	V_{ESD-1}	± 17	kV
ESD per IEC 61000-4-2 (Contact)	V_{ESD-2}	± 17	
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	$^{\circ}C$
Operating Temperature	T_{OP}	-55 to +125	$^{\circ}C$
Storage Temperature	T_{STO}	-55 to +150	$^{\circ}C$

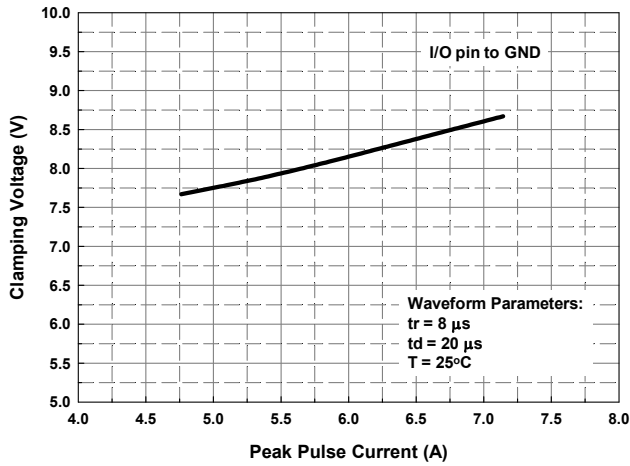
Electrical Characteristics						
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V_{RWM}	Pin-1,-2 to pin-3, $T = 25^{\circ}C$.			5	V
Channel Leakage Current	$I_{CH-Leak}$	$V_{RWM} = 5V$, $T = 25^{\circ}C$, pin-1,-2 to pin-3.			1	μA
Reverse Breakdown Voltage	V_{BV}	$I_{BV} = 1mA$, $T = 25^{\circ}C$, pin-1,-2 to pin-3.	6		9	V
Forward Voltage	V_F	$I_F = 15mA$, $T = 25^{\circ}C$, pin-3 to pin-1,-2.		0.8	1.2	V
ESD Clamping Voltage (Note 1)	V_{CL-ESD}	IEC 61000-4-2 +8kV ($I_{TLP} = 16A$), $T = 25^{\circ}C$, contact mode, any I/O pin to GND.		10.5		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+8kV, $T = 25^{\circ}C$, contact mode, any I/O pin to GND.		0.25		Ω
Surge Clamping Voltage	$V_{CL-surge}$	$I_{PP} = 5A$, $t_p = 8/20\mu s$, $T = 25^{\circ}C$, any I/O pin to GND.		7.7		V
Channel Input Capacitance	C_{IN}	$V_{Pin-3} = 0V$, $V_{IN} = 2.5V$, $f = 1MHz$, $T = 25^{\circ}C$, any I/O pin to GND.		2	2.5	pF
Channel to Channel Input Capacitance	$C_{I/O-to-I/O}$	$V_{Pin-3} = 0V$, $V_{IN} = 2.5V$, $f = 1MHz$, $T = 25^{\circ}C$, between I/O pins.		0.3	0.4	pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

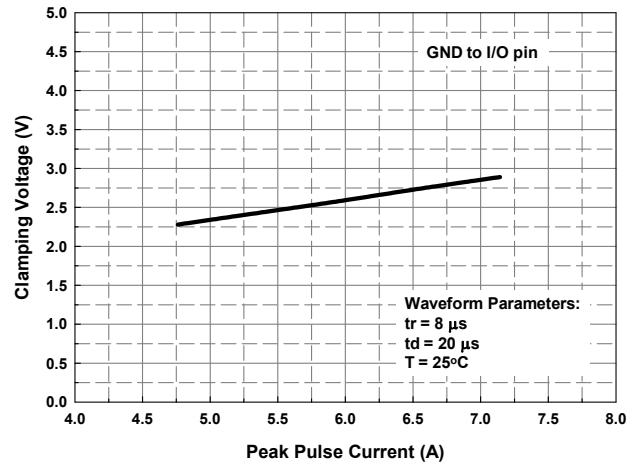
TLP conditions: $Z_0 = 50\Omega$, $t_p = 100ns$, $t_r = 1ns$.

Typical Characteristics

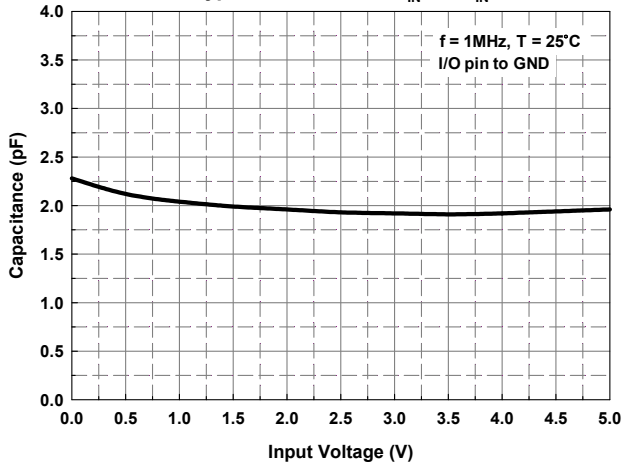
Reverse Clamping Voltage vs. Peak Pulse Current



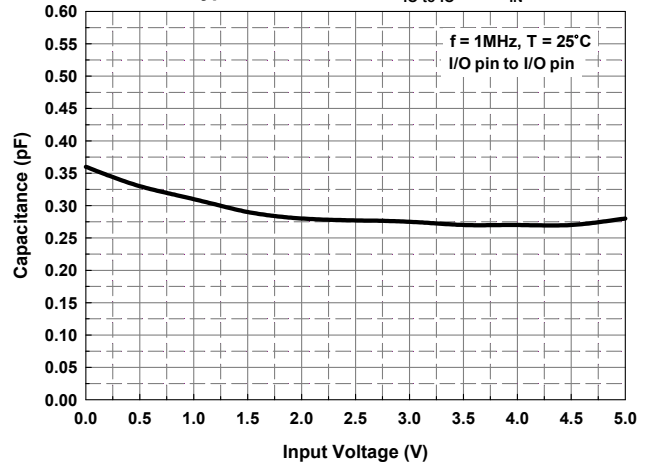
Forward Clamping Voltage vs. Peak Pulse Current



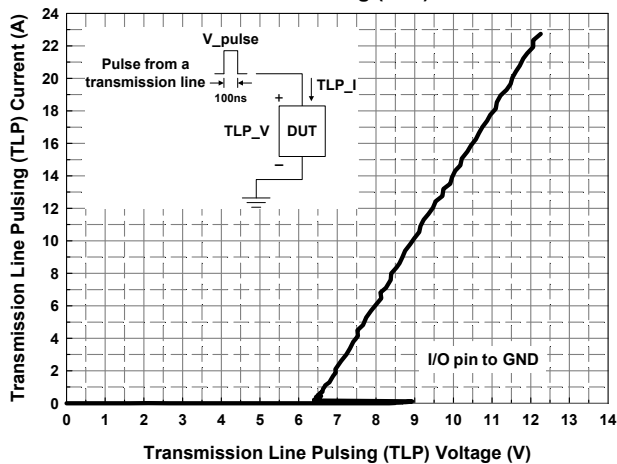
Typical Variation of C_{IN} vs. V_{IN}



Typical Variation of $C_{IO-to-IO}$ vs. V_{IN}



Transmission Line Pulsing (TLP) Measurement



Applications Information

The AZ9C39-02S is designed to protect two lines against system ESD pulses by clamping them to an acceptable reference.

The usage of the AZ9C39-02S is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin 1 and 2. The pin 3 should be connected directly to a ground plane on the board. All path lengths connected to the pins of AZ9C39-02S should be kept as short as possible to minimize parasitic inductance in the board traces.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ9C39-02S.
- Place the AZ9C39-02S near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

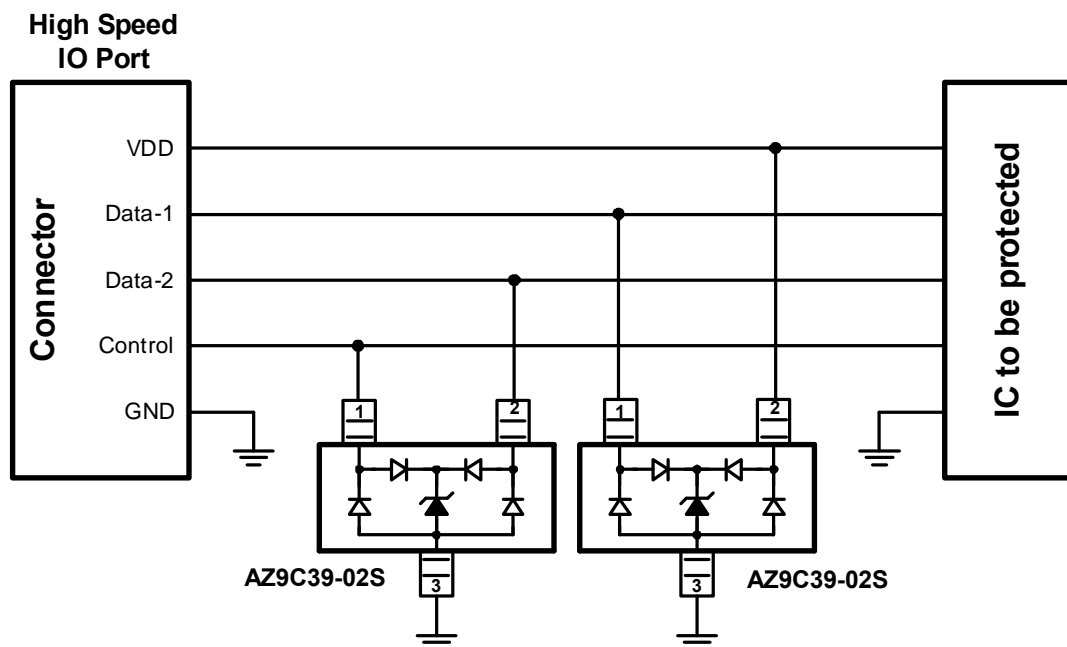
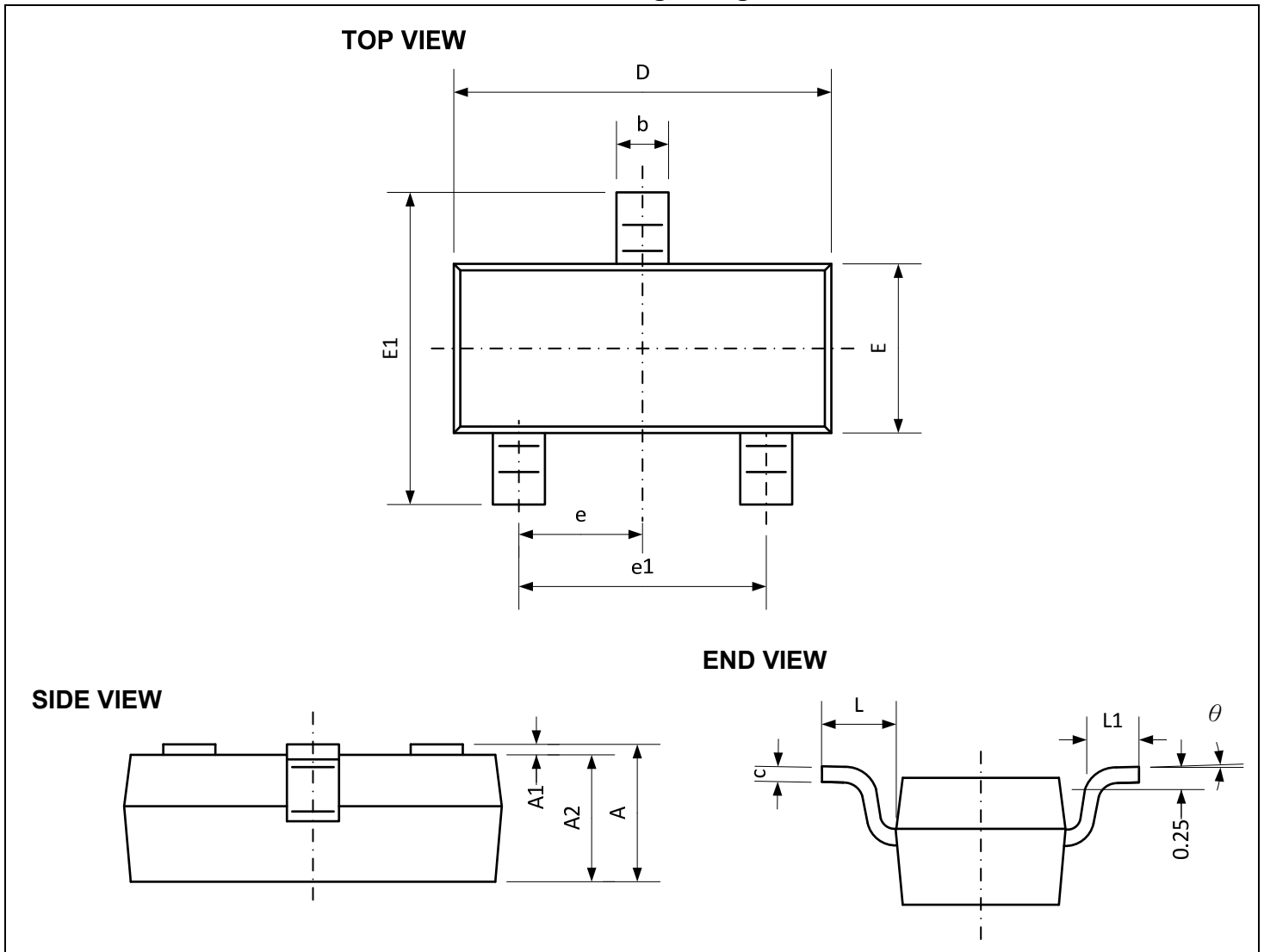


Fig. 1 High speed IO port ESD protection by using AZ9C39-02S.

Mechanical Details

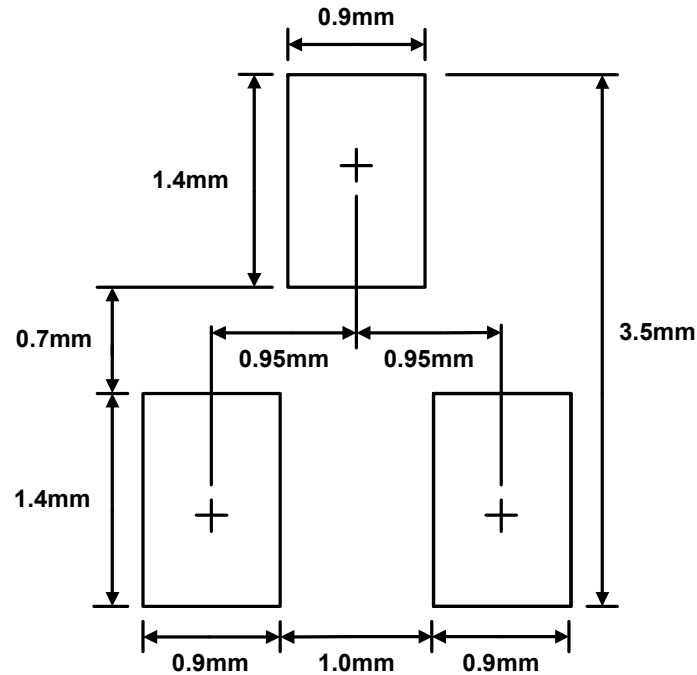
SOT23-3L Package Diagrams



Package Dimensions

SYMBOL	MILLIMETERS		SYMBOL	MILLIMETERS		SYMBOL	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.		MIN.	MAX.
A	0.90	1.15	D	2.80	3.00	L	0.55 REF	
A1	0.00	0.10	E	1.20	1.40	L1	0.30	0.50
A2	0.90	1.05	E1	2.25	2.55	θ	0	8
b	0.30	0.50	e	0.95 TYP				
c	0.08	0.15	e1	1.80	2.00			

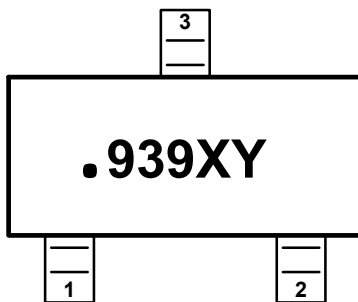
Land Layout



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

Marking Code



939 = Device Code
X = Date Code
Y = Control Code

Part Number	Marking Code
AZ9C39-02S.R7G (Green part)	939XY

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ9C39-02S.R7G	Green	T/R	7 inch	3,000/reel	4 reels= 12,000/box	6 boxes= 72,000/carton



Revision History

Revision	Modification Description
Revision 2022/05/06	Formal Release.