

Features

- ESD/Surge protection for two lines with bi-directional
- Provide transient protection for each line to **IEC 61000-4-2 (ESD) $\pm 20\text{kV}$ (air), $\pm 20\text{kV}$ (contact) IEC 61000-4-5 (Lightning) 2A (8/20 μs)**
- Suitable for, 36V and below, operating voltage applications
- Fast turn-on and low clamping voltage
- Array of ESD rated equivalent TVS diodes
- Small package saves board space
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green part**
- **AEC-Q101 qualified**

Applications

- Automotive network protection:
 - CAN/CAN-FD
 - FlexRay
- Industrial control
- Power management system
- Set-top box
- Notebooks, desktops, and servers
- Portable instrumentation
- Peripherals

Description

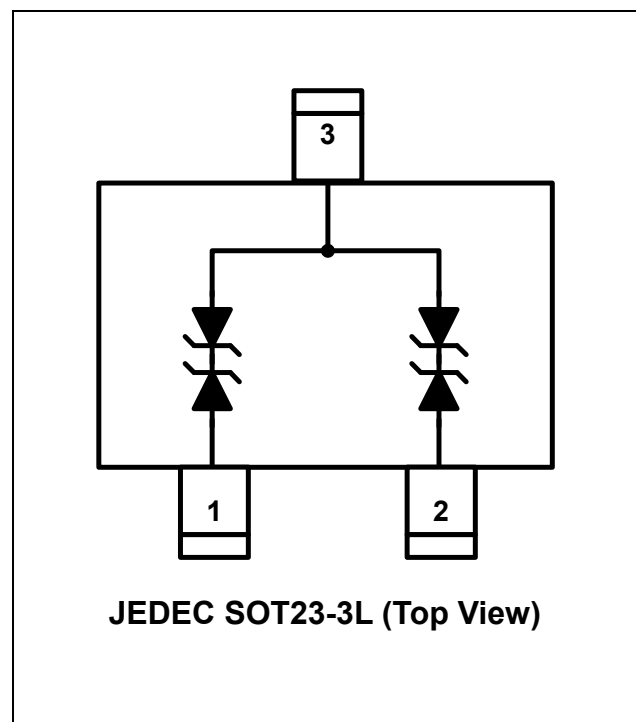
AZ9436-02S is a design which includes ESD /surge rated clamping cell arrays to protect the data lines, control lines or power lines in an electronic system. The AZ9436-02S has been specifically designed to protect sensitive components which are connected to data lines,

control lines or power lines from over-voltage caused by Electrostatic Discharging (ESD), Lightning, and Cable Discharge Event (CDE).

AZ9436-02S is a unique design which includes proprietary clamping cells in a single package. During transient conditions, the proprietary clamping cells prevent over-voltage on the data lines, control lines or power lines, protecting any downstream components.

AZ9436-02S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Circuit Diagram / Pin Configuration



Specifications

Absolute Maximum Ratings			
Parameter	Symbol	Rating	Unit
Peak Pulse Current ($t_p=8/20\mu s$)	I_{PP} (Note 1)	2	A
Operating Voltage (I/O pin-GND)	V_{DC}	± 38	V
ESD per IEC 61000-4-2 (Air)	V_{ESD-1}	± 20	kV
ESD per IEC 61000-4-2 (Contact)	V_{ESD-2}	± 20	
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	$^{\circ}C$
Operating Temperature	T_{OP}	-55 to +150	$^{\circ}C$
Storage Temperature	T_{STO}	-55 to +150	$^{\circ}C$

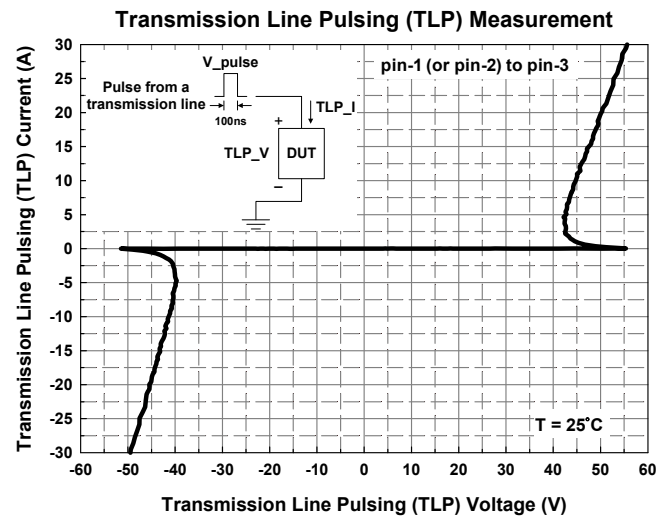
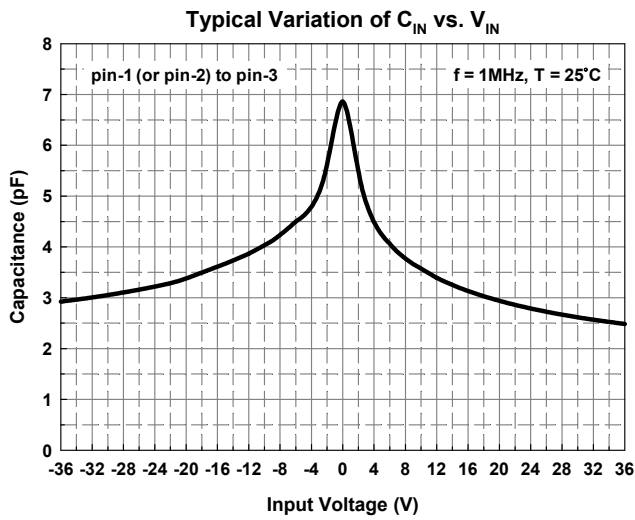
Electrical Characteristics						
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V_{RWM}	Pin-1, -2 to pin-3, $T=25^{\circ}C$.	-36		36	V
Reverse Leakage Current	I_{Leak}	$V_{RWM} = \pm 36V$, pin-1, -2 to pin-3, $T=25^{\circ}C$.			1	μA
Reverse Breakdown Voltage	V_{BV}	$I_{BV} = 1mA$, pin-1, -2 to pin-3, $T=25^{\circ}C$.	40			V
Surge Clamping Voltage (Note 1)	$V_{CL-Surge}$	$I_{PP} = 2A$, $t_p = 8/20\mu s$, pin-1, -2 to pin-3, $T = 25^{\circ}C$.		50		V
ESD Clamping Voltage (Note 2)	V_{CL-ESD}	IEC 61000-4-2 +8kV ($I_{TLP} = 16A$), contact mode, pin-1, -2 to pin-3, $T=25^{\circ}C$.		50		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+8kV, contact mode, pin-1, -2 to pin-3, $T=25^{\circ}C$.		0.5		Ω
Channel Input Capacitance	C_{IN}	$V_R = 2.5V$, $f = 1MHz$, pin-1, -2 to pin-3, $T=25^{\circ}C$.		5.2	6.5	pF
		$V_R = 2.5V$, $f = 1MHz$, pin-1, -2 to pin-3, $T=150^{\circ}C$.			8	pF

Note 1: The Peak Pulse Current measured conditions: $t_p = 8/20\mu s$, 2Ω source impedance.

Note 2: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions: $Z_0 = 50\Omega$, $t_p = 100ns$, $t_r = 1ns$

Typical Characteristics



Application Information

The AZ9436-02S is designed to protect two lines against system ESD/Lightning pulses by clamping it to an acceptable reference.

The usage of the AZ9436-02S is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected to pin 1 and pin 2, respectively. The pin 3 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ9436-02S should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, a good circuit board is

critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ9436-02S.
- Place the AZ9436-02S near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

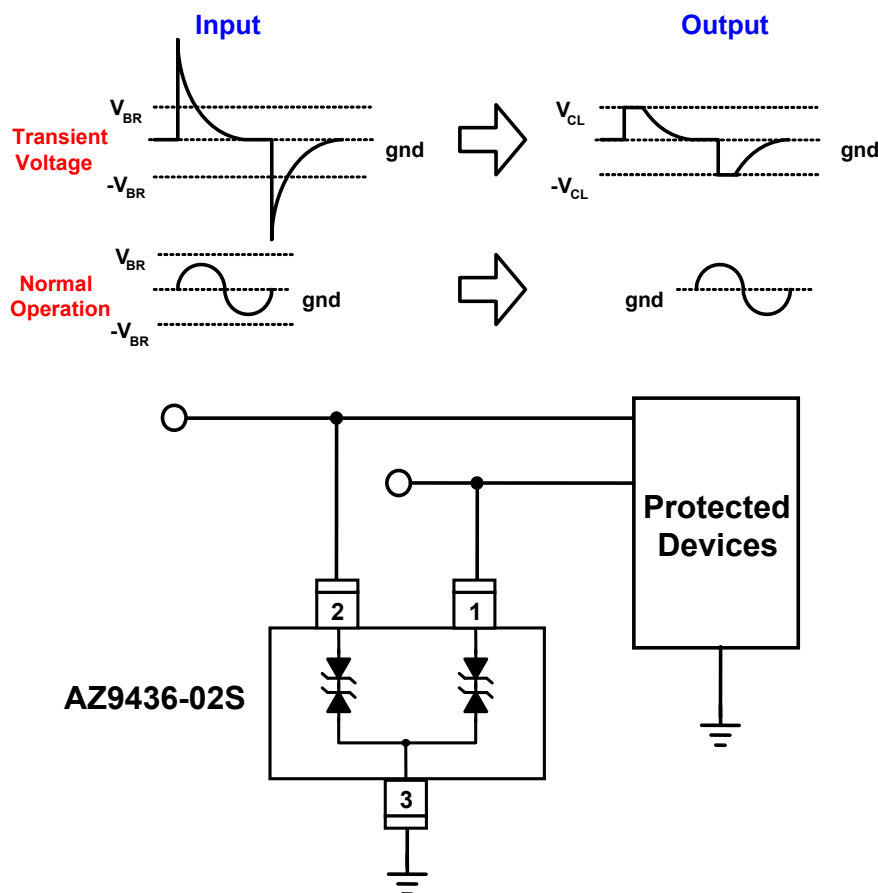
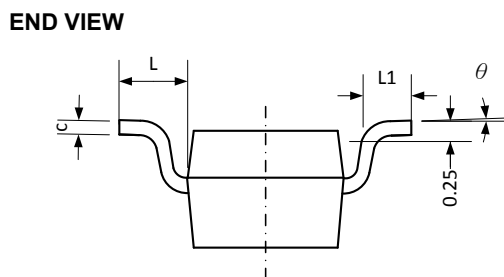
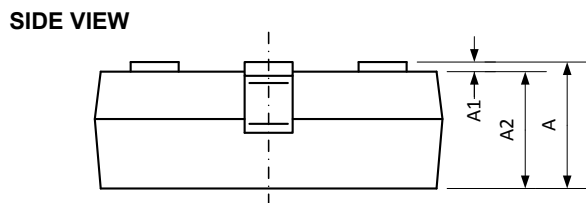
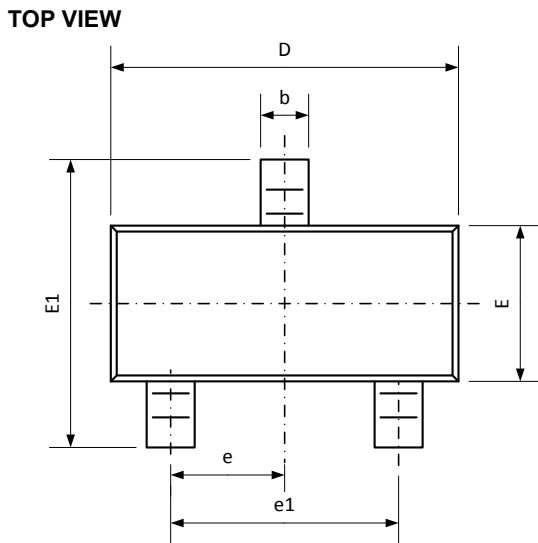


Fig. 1 The ESD protection scheme by using AZ9436-02S.

Mechanical Details

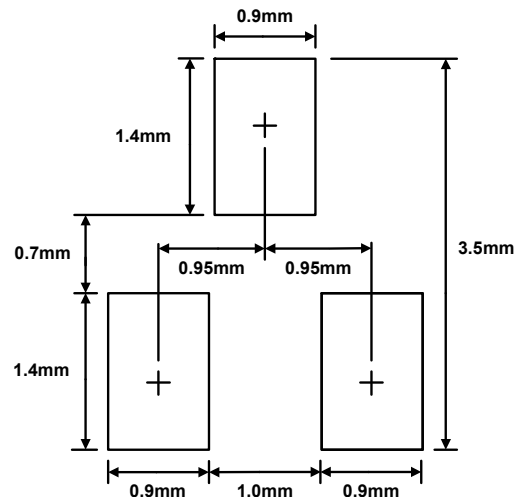
SOT23-3L Package Diagrams



Package Dimensions

Symbol	Millimeters	
	Min	Max
A	0.89	1.15
A1	0.00	0.10
A2	0.88	1.05
b	0.30	0.50
c	0.08	0.15
D	2.80	3.00
E	1.20	1.40
E1	2.25	2.63
e	0.95 TYP	
e1	1.80	2.00
L	0.58 REF	
L1	0.30	0.60
θ	0	8

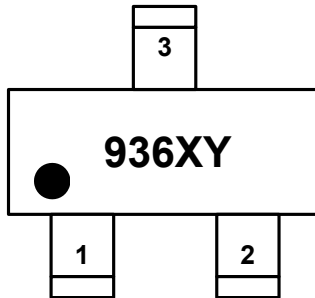
Land Layout



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

Marking Code



936 = Device Code
X = Date Code
Y = Control Code

Part Number	Marking Code
AZ9436-02S.R7G (Green Part)	936XY

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ9436-02S.R7G	Green	T/R	7 inch	3,000/reel	4 reels=12,000/box	6 boxes=72,000/carton

Revision History

Revision	Modification Description
Revision 2024/08/15	Preliminary Release.
Revision 2025/07/25	Formal Release.