

Features

- ESD/Surge protection for 1 line with bi-directional
- Provide transient protection for each line to
IEC 61000-4-2 (ESD) $\pm 30\text{kV}$ (air / contact)
IEC 61000-4-4 (EFT) $\pm 80\text{A}$ (5/50ns)
IEC 61000-4-5 (Lightning) 16A (8/20 μs)
- Suitable for, **5V and below**, operating voltage applications
- **0201 small MCSP package** saves board space
- Protect one I/O line or one power line
- Fast turn-on and low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green part**

Applications

- Cellular handsets and accessories
- Power supply protection
- Small panel modules
- Handheld portable applications
- Low speed data or control line protection
- Peripherals
- Consumer electronics

Description

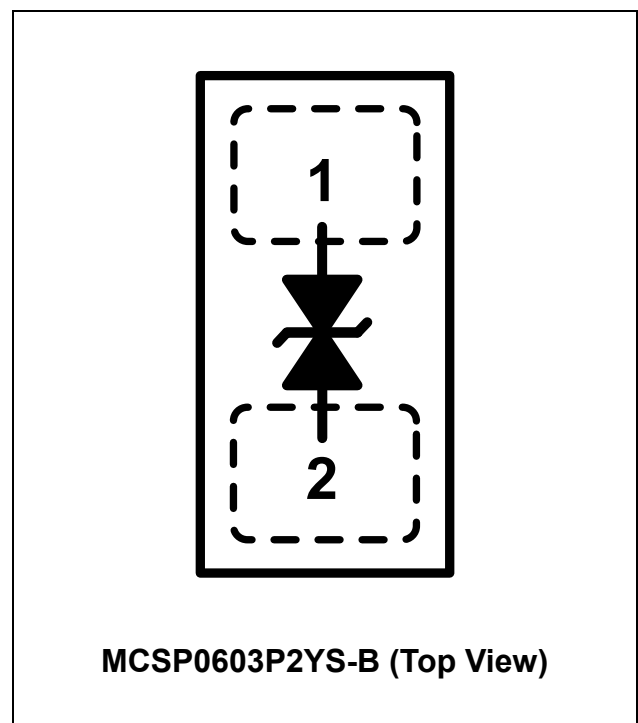
AZ5A05-01M is a design which includes a bi-directional surge rated clamping cell to protect one power line, or one control line, or one low speed data line in an electronic system. The AZ5A05-01M has been specifically designed to protect sensitive components which are connected to power and control lines from

over-voltage damage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ5A05-01M is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ5A05-01M may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Circuit Diagram / Pin Configuration



Specifications

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$, unless otherwise specified)			
Parameter	Symbol	Rating	Unit
Peak Pulse Current ($t_p = 8/20\mu\text{s}$)	I_{PP} (Note 1)	16	A
Operating Voltage	V_{DC}	± 5.5	V
ESD per IEC 61000-4-2 (Air)	V_{ESD-1}	± 30	kV
ESD per IEC 61000-4-2 (Contact)	V_{ESD-2}	± 30	
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	$^\circ\text{C}$
Operating Temperature	T_{OP}	-55 to +125	$^\circ\text{C}$
Storage Temperature	T_{STO}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics						
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V_{RWM}	$T = 25^\circ\text{C}$.	-5		5	V
Reverse Leakage Current	I_{Leak}	$V_{RWM} = \pm 5\text{V}$, $T = 25^\circ\text{C}$.			100	nA
Reverse Breakdown Voltage	V_{BV}	$I_{BV} = 1\text{mA}$, $T = 25^\circ\text{C}$.	6		9	V
Surge Clamping Voltage (Note 1)	$V_{CL-surge}$	$I_{PP} = 5\text{A}$, $t_p = 8/20\mu\text{s}$, $T = 25^\circ\text{C}$.		8.3	9.5	V
		$I_{PP} = 10\text{A}$, $t_p = 8/20\mu\text{s}$, $T = 25^\circ\text{C}$.		9.2	10.5	
		$I_{PP} = 16\text{A}$, $t_p = 8/20\mu\text{s}$, $T = 25^\circ\text{C}$.		10.2	12	
ESD Clamping Voltage (Note 2)	V_{CL-ESD}	IEC 61000-4-2 +8kV ($I_{TLP} = 16\text{A}$), contact mode, $T = 25^\circ\text{C}$.		9.5		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2 +6~+30kV, $T = 25^\circ\text{C}$, contact mode.		0.07		Ω
Channel Input Capacitance	C_{IN}	$V_R = 0\text{V}$, $f = 1\text{MHz}$, $T = 25^\circ\text{C}$.		9	12	pF

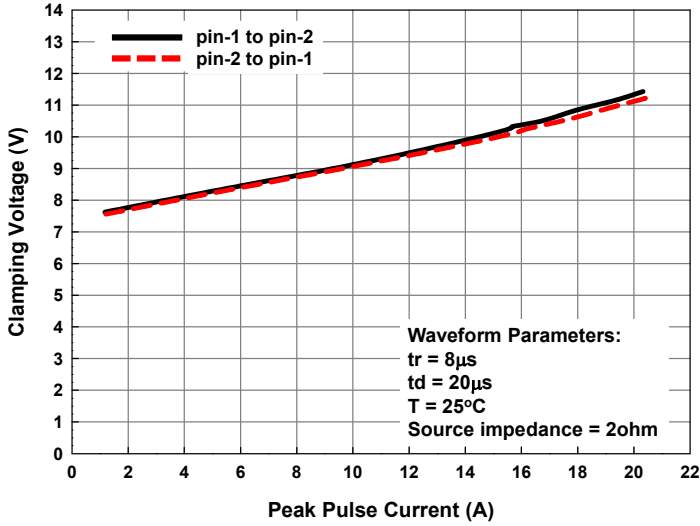
Note 1: The Peak Pulse Current measured conditions: $t_p = 8/20\mu\text{s}$, 2Ω source impedance.

Note 2: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

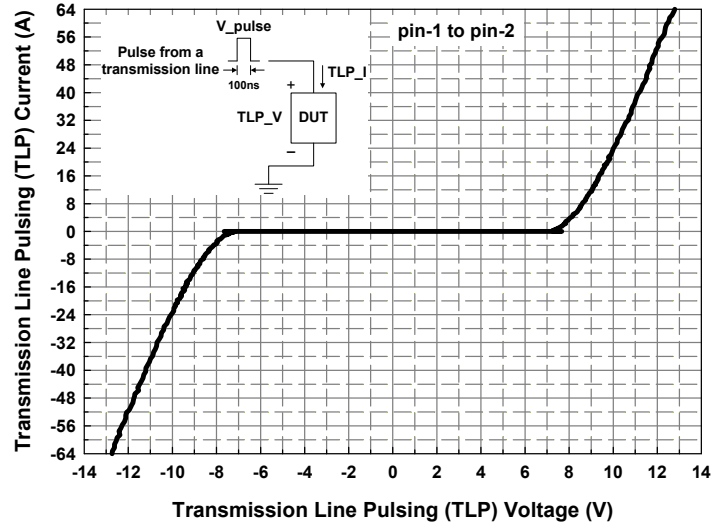
TLP conditions: $Z_0 = 50\Omega$, $t_p = 100\text{ns}$, $t_r = 1\text{ns}$.

Typical Characteristics

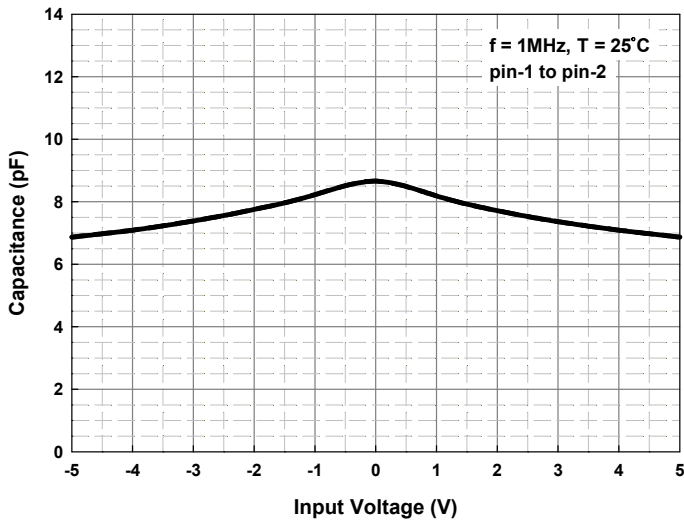
Reverse Clamping Voltage vs. Peak Pulse Current



Transmission Line Pulsing (TLP) Measurement



Typical Variation of C_{IN} vs. V_{IN}



Applications Information

The AZ5A05-01M is designed to protect one line against system ESD/EFT/Lightning pulses by clamping it to an acceptable reference.

The usage of the AZ5A05-01M is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected to pin-1. The pin-2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ5A05-01M should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ5A05-01M.
- Place the AZ5A05-01M near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

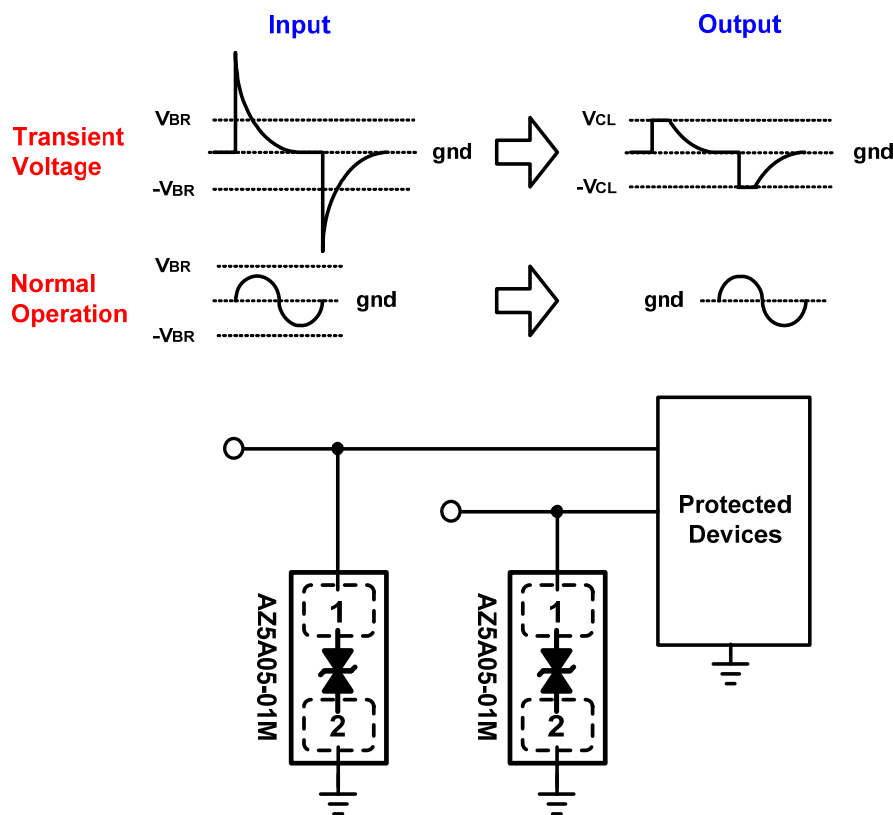


Fig. 1

Fig. 2 shows another simplified example of using AZ5A05-01M to protect the control line, low speed data line, and power line from ESD transient stress.

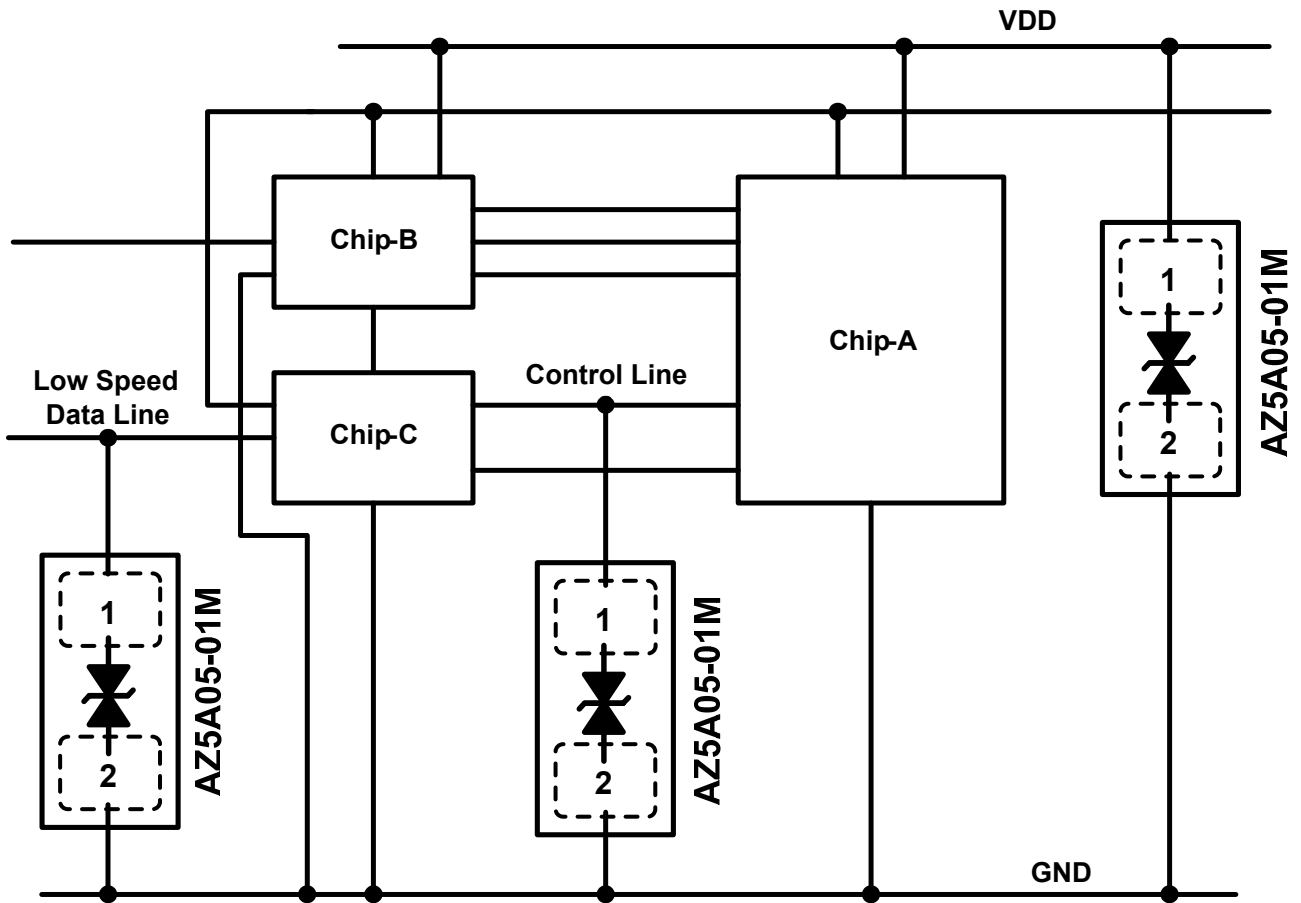
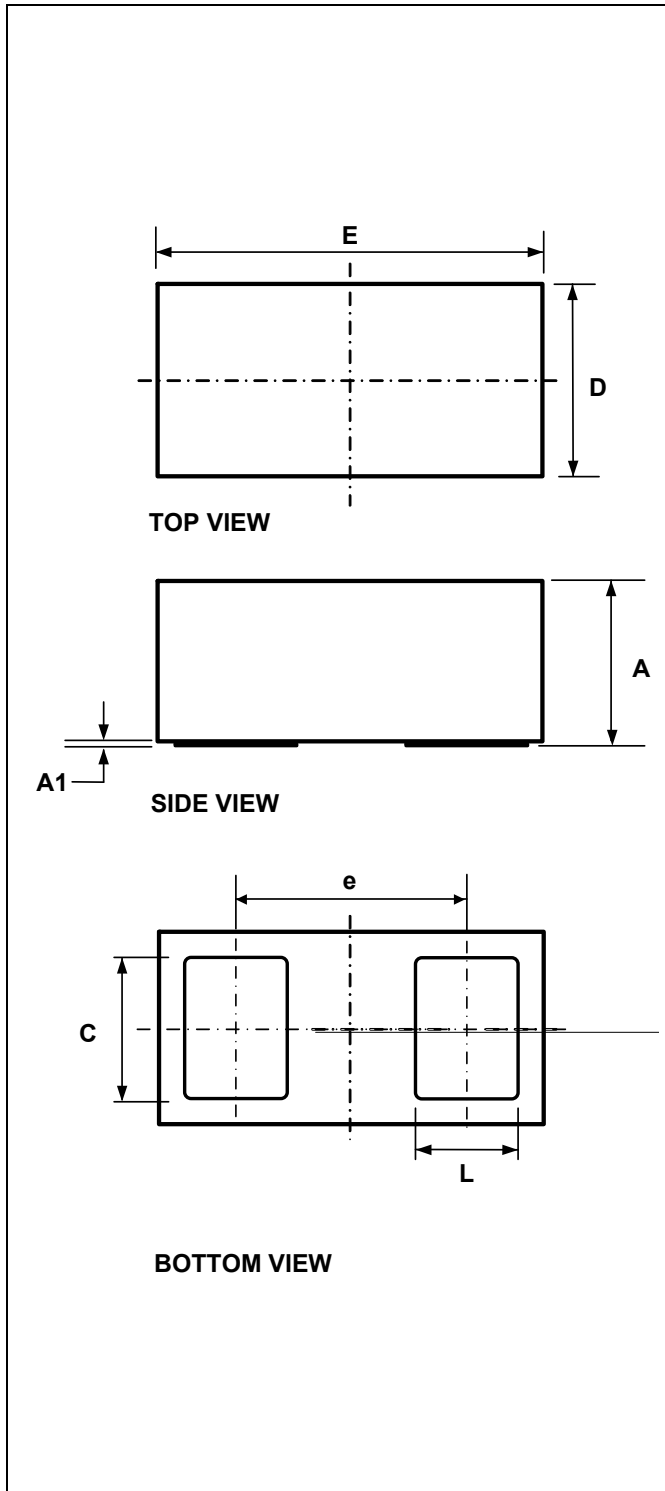


Fig. 2

Mechanical Details

MCSP0603P2YS-B

Package Diagrams

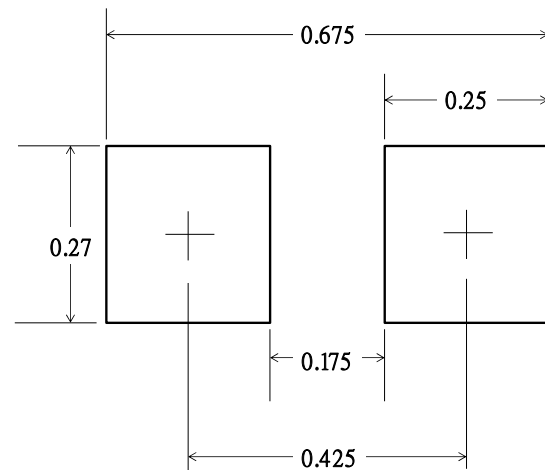


Package Dimensions

SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
E	0.580	0.600	0.620
D	0.280	0.300	0.320
A	0.235	0.250	0.265
A1	0.000	0.010	0.050
L	0.140	0.160	0.180
C	0.200	0.220	0.240
e	0.360 BSC		

Land Layout

Unit: mm

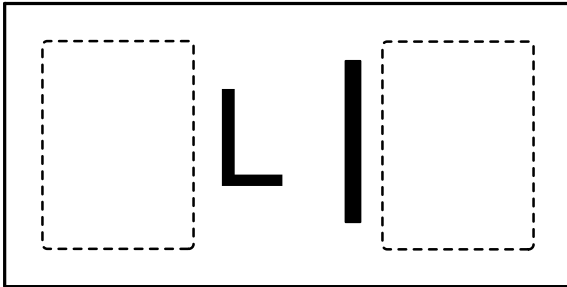


Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.



Marking Code



L= Device Code

Part Number	Marking Code
AZ5A05-01M.R7G (Green Part)	L

Note : Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ5A05-01M.R7G	Green	T/R	7 inch	15,000/reel	4 reels = 60,000/box	6 boxes = 360,000/carton

Revision History

Revision	Modification Description
Revision 2024/06/19	Preliminary Release.
Revision 2024/08/21	Formal Release.