



## Features

- ESD Protection for 1 line with Bi-directional
- Provide ESD protection for the protected line to  
**IEC 61000-4-2 (ESD)  $\pm 30\text{kV}$  (air / contact)**  
**IEC 61000-4-4 (EFT) 80A (5/50ns)**  
**IEC 61000-4-5 (Lightning) 80A (8/20 $\mu\text{s}$ )**
- For low operating voltage applications: 2.5V
- DFN package saves board space
- Protect one I/O line or power line
- Fast turn-on and Low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green Part**

## Applications

- Mobile Phones
- Hand Held Portable Applications
- Computer Interfaces Protection
- Microprocessors Protection
- Serial and Parallel Ports Protection
- Control Signal Lines Protection
- Power lines on PCB Protection
- 2.5V operating systems

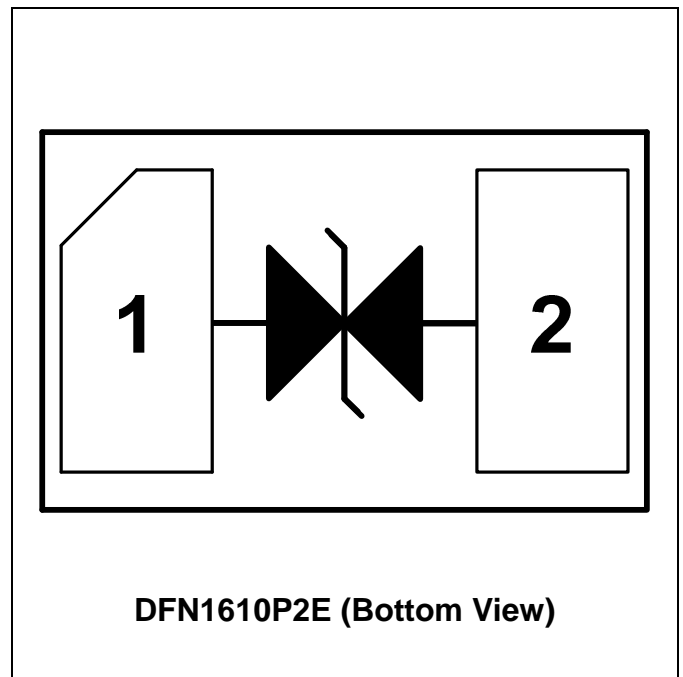
## Description

AZ6425-01F is a design which includes one bi-directional surge rated clamping cell to protect one power line, or one control line, or one low speed data line in an electronic systems. The AZ6425-01F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ6425-01F is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ6425-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ( $\pm 15\text{kV}$  air,  $\pm 8\text{kV}$  contact discharge).

## Circuit Diagram / Pin Configuration





## SPECIFICATION

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	SYMBOL	RATING	UNITS
Peak Pulse Current (tp = 8/20μs)	I <sub>PP</sub>	80	A
Operating Supply Voltage	V <sub>DC</sub>	±2.8	V
ESD per IEC 61000-4-2 (Air)	V <sub>ESD</sub>	±30	kV
ESD per IEC 61000-4-2 (Contact)		±30	
Lead Soldering Temperature	T <sub>SOL</sub>	260 (10 sec.)	°C
Operating Temperature	T <sub>OP</sub>	-55 to +85	°C
Storage Temperature	T <sub>STO</sub>	-55 to +150	°C

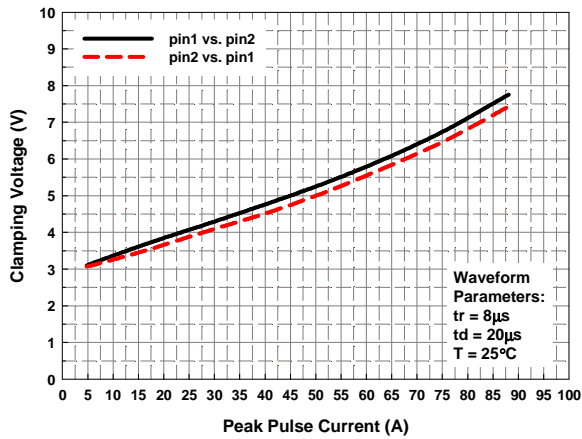
ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MINI	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V <sub>RWM</sub>	T= 25°C.	-2.5		2.5	V
Reverse Leakage Current	I <sub>Leak</sub>	V <sub>RWM</sub> = ±2.5V, T= 25°C.			2	μA
Reverse Breakdown Voltage	V <sub>BV</sub>	I <sub>BV</sub> = 1mA, T= 25°C.	3.5			V
Surge Clamping Voltage	V <sub>CL-surge</sub>	I <sub>PP</sub> = 5A, tp = 8/20μs, T= 25°C.		3.0		V
		I <sub>PP</sub> = 80A, tp = 8/20μs, T= 25°C.		7.0		
ESD Clamping Voltage (Note 1)	V <sub>clamp</sub>	IEC 61000-4-2 +8kV (I <sub>TLP</sub> = 16A), Contact mode, T= 25°C.		4.0		V
ESD Dynamic Turn-on Resistance	R <sub>dynamic</sub>	IEC 61000-4-2 0~+8kV, Contact mode, T= 25°C.		0.03		Ω
Channel Input Capacitance	C <sub>IN</sub>	V <sub>R</sub> = 0V, f = 1MHz, T=25°C.		355	390	pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

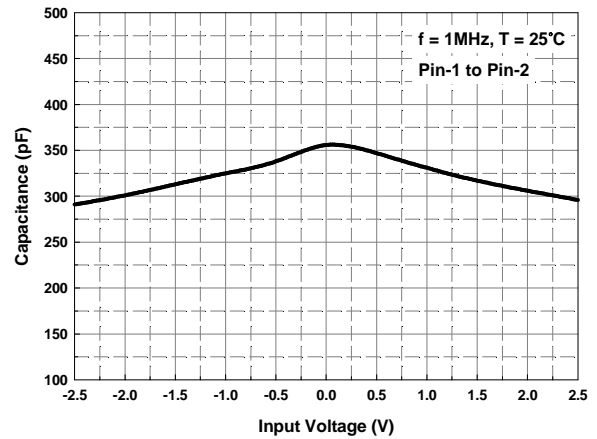
TLP conditions: Z<sub>0</sub>= 50Ω, t<sub>p</sub>= 100ns, t<sub>r</sub>= 1ns.

## Typical Characteristics

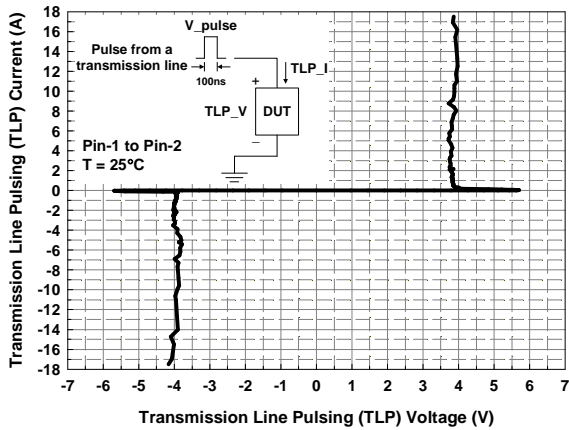
Reverse Clamping Voltage vs. Peak Pulse Current



Typical Variation of  $C_{IN}$  vs.  $V_{IN}$



Transmission Line Pulsing (TLP) Measurement



## Applications Information

The AZ6425-01F is designed to protect one line against System ESD/EFT/Surge pulses by clamping them to an acceptable reference. It provides bi-directional protection.

The usage of the AZ6425-01F is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ6425-01F should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ6425-01F.
- Place the AZ6425-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

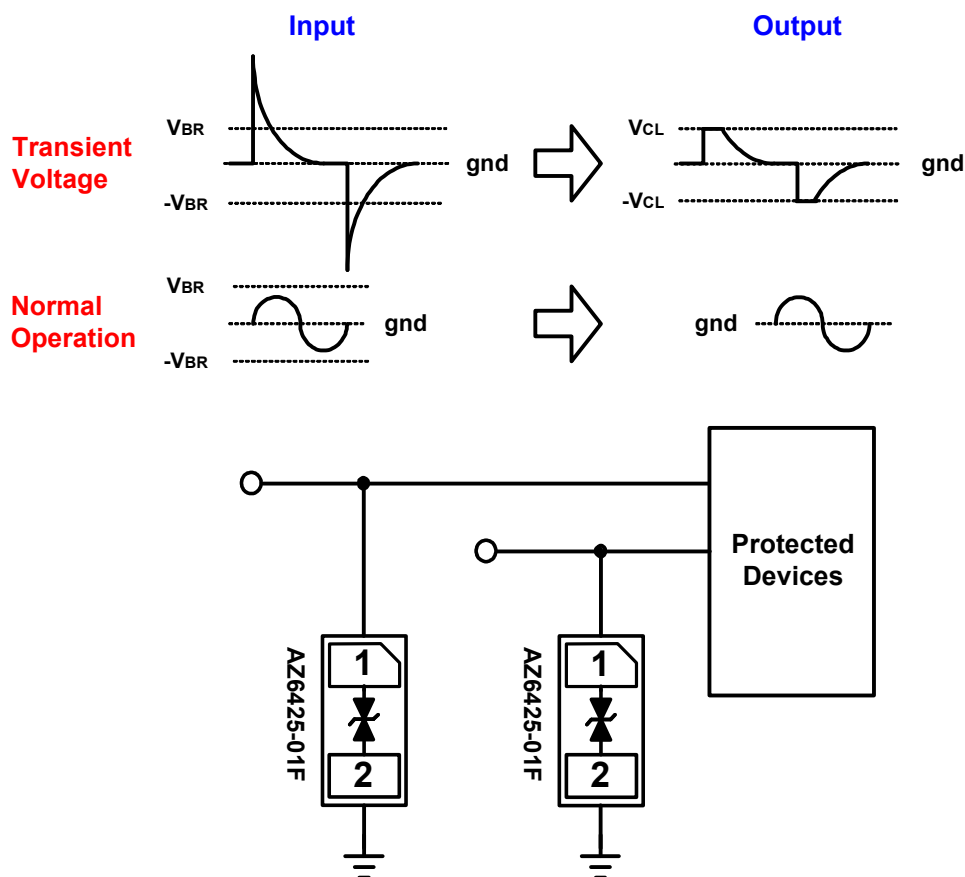
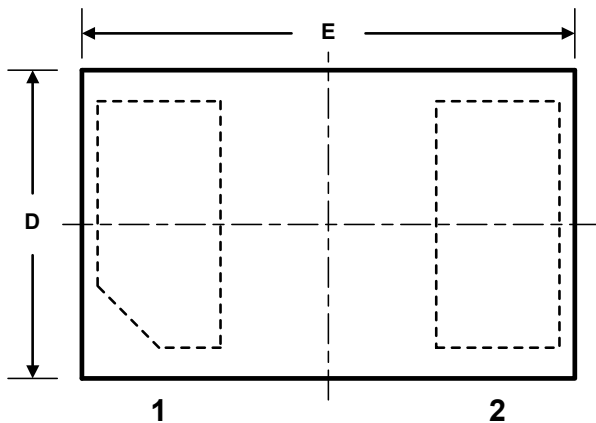


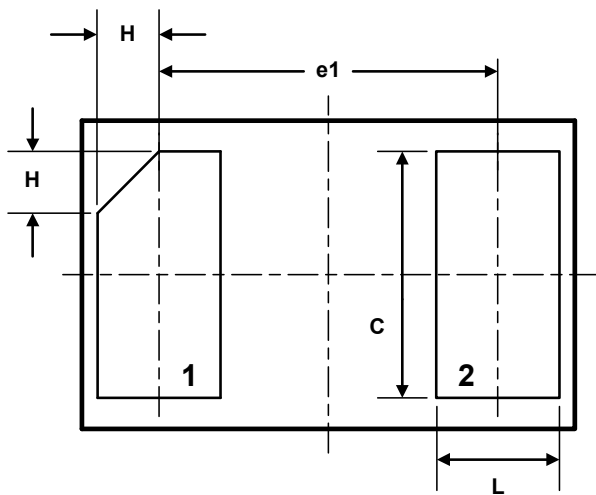
Fig. 1 ESD protection scheme by using AZ6425-01F.

## Mechanical Details

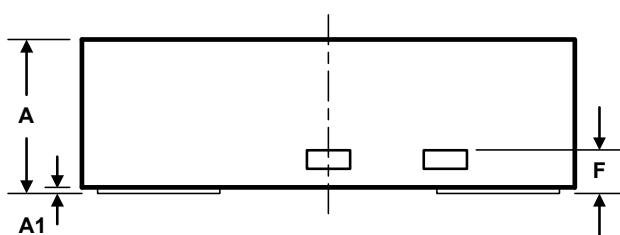
### DFN1610P2E PACKAGE DIAGRAMS



Top View



Bottom View

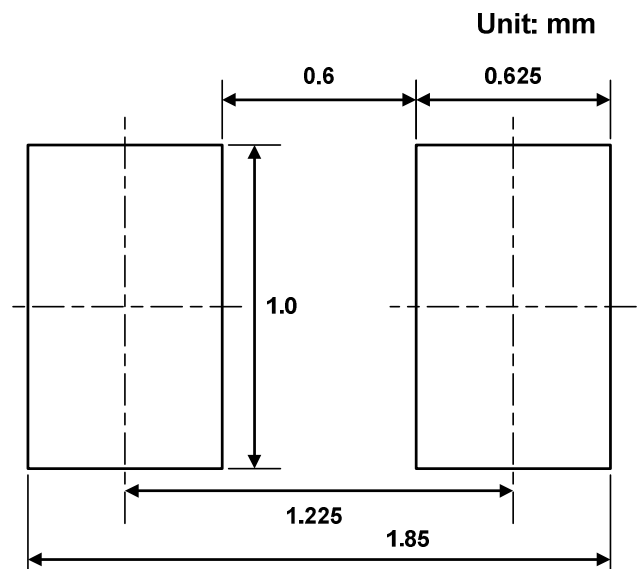


Side View

### PACKAGE DIMENSIONS

SYMBOL	Millimeter		
	Min.	Typ.	Max.
D	0.95	1.00	1.05
E	1.55	1.60	1.65
C	0.75	0.80	0.85
A	0.45	0.50	0.55
A1	-	0.02	0.05
e1	1.10BSC		
F	0.10	0.15	0.20
H	0.15	0.20	0.25
L	0.35	0.40	0.45

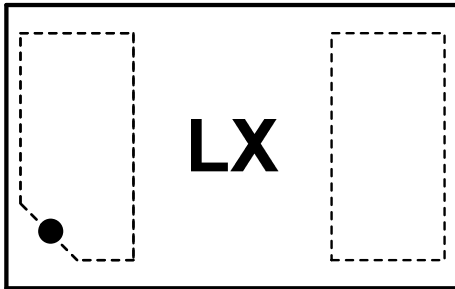
### LAND LAYOUT



#### Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

## MARKING CODE



**Top View**

Part Number	Marking Code
AZ6425-01F.R7G (Green Part)	LX

Note. Green means Pb-free, RoHS, and Halogen free compliant.

L = Device Code  
X = Date Code

## Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ6425-01F.R7G	Green	T/R	7 inch	3,000/reel	4 reels = 12,000/box	6 boxes = 72,000/carton

## Revision History

Revision	Modification Description
Revision 2016/10/18	Preliminary Release.
Revision 2017/03/20	Formal Release.