Features

- ESD Protection for 1 line with Uni-directional
- Provide ESD protection for the protected line to
  IEC 61000-4-2 (ESD) ±15kV (air/contact)
  IEC 61000-4-4 (EFT) 80A (5/50ns)
  IEC 61000-4-5 (Lightning) 12A (8/20μs)
- For low operating voltage applications: **1.2V**
- **Fast turn-on and Ultra-low clamping voltage**
- **Active circuit triggering technology**
- **0402 small DFN package** saves board space
- Protect one I/O line or one power line
- ***Green Part***

Applications

- Mobiles Phones
- Hand Held Portable Applications
- Computer Interfaces Protection
- Microprocessors Protection
- Serial and Parallel Ports Protection
- Control Signal Lines Protection
- Power lines on PCB Protection
- Latchup Protection

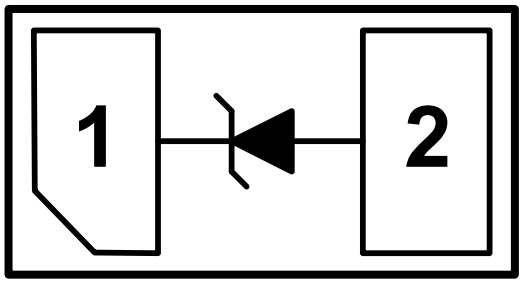
Description

AZ6112-01F is a design which includes one Uni-directional ESD rated clamping cell to protect one power line, or one control line, or one low speed data line in an electronic systems. The AZ6112-01F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ6112-01F is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ6112-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge)

Circuit Diagram / Pin Configuration



DFN1006P2E (Bottom View)

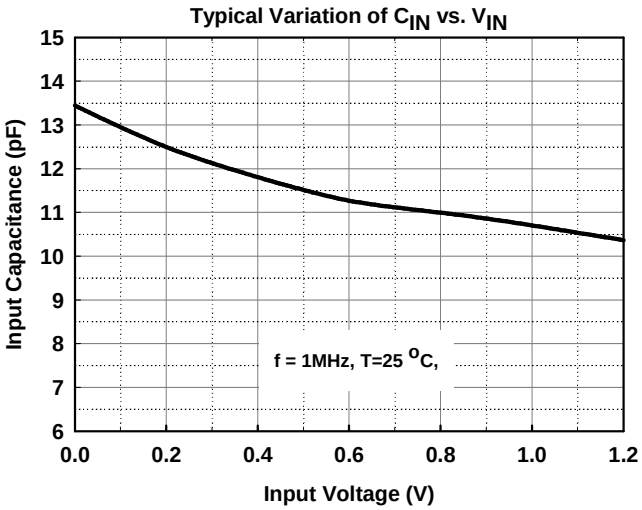
SPECIFICATIONS

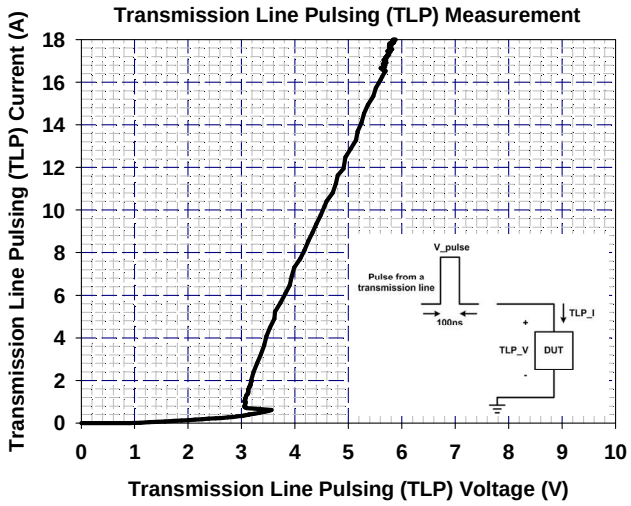
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**SYMBOL**	**RATING**	**UNITS**
Peak Pulse Current (tp=8/20μs)	I_{PP}	12	A
Operating Supply Voltage (pin-1 to pin-2)	V_{DC}	1.32	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±15 ±15	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +85	°C
Storage Temperature	T_{STO}	-55 to +150	°C

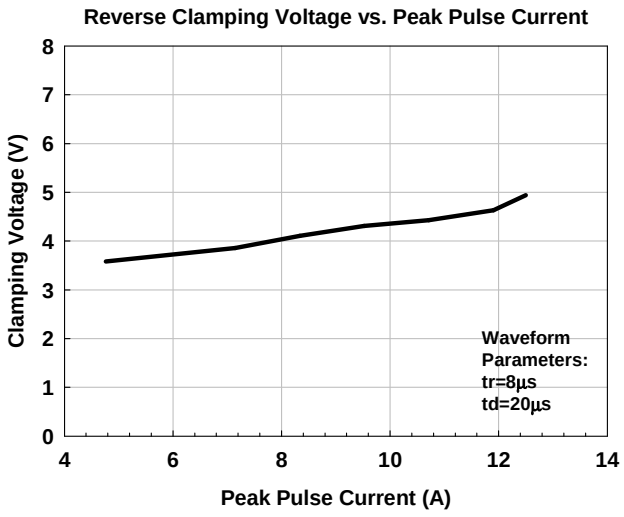
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MINI**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	T=25 °C.			1.2	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = 1.2V, T=25 °C.			0.5	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C.		11		V
Forward Voltage	V_F	I_F = 15mA, T=25 °C.	0.6		1.0	V
ESD Trigger Voltage (Note 1)	$V_{ESD\_trigger}$	IEC 61000-4-2, T=25 °C, Contact mode.		3.5		V
ESD Clamping Voltage (Note 1)	V_{ESD_CL}	IEC 61000-4-2 +2kV (I_{TLP}=4A), T=25 °C, Contact mode.		3.2		V
		IEC 61000-4-2 +4kV (I_{TLP}=8A), T=25 °C, Contact mode.		4.0		V
		IEC 61000-4-2 +6kV (I_{TLP}=12A), T=25 °C, Contact mode.		5.0		V
Channel Input Capacitance	C_{IN}	V_R = 0V, f = 1MHz, T=25 °C.		13.5	20	pF

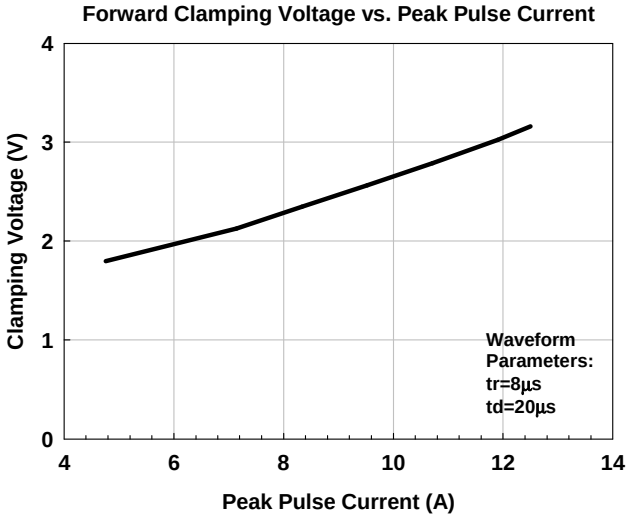
Note 1: ESD Trigger Voltage and ESD Clamping Voltage were measured by Transmission Line Pulsing (TLP) System.
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 2ns.

Typical Characteristics









Applications Information

The AZ6112-01F is designed to protect one line against System ESD/EFT/Lightning pulses by clamping it to an acceptable reference. It provides unidirectional protection.

The usage of the AZ6112-01F is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin2 should be connected directly to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ6112-01F should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ6112-01F.
- Place the AZ6112-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

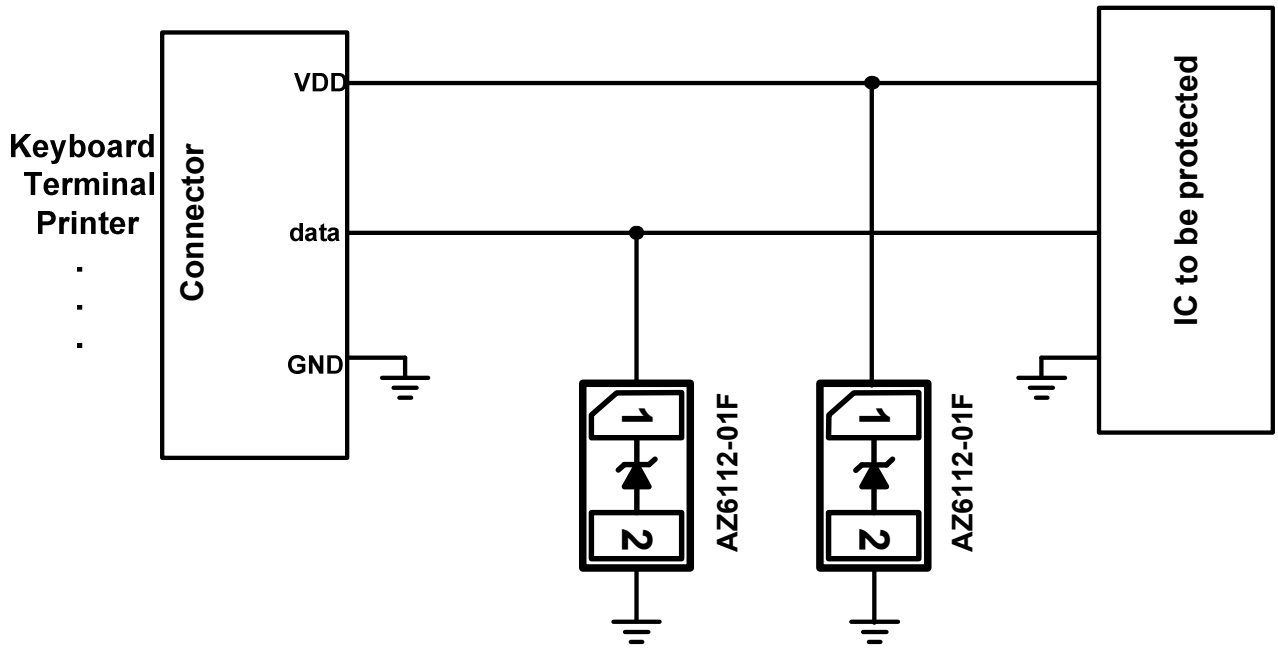


Fig. 1

Fig. 2 shows another simplified example of using AZ6112-01F to protect the control lines, low speed data lines, and power lines from ESD transient stress.

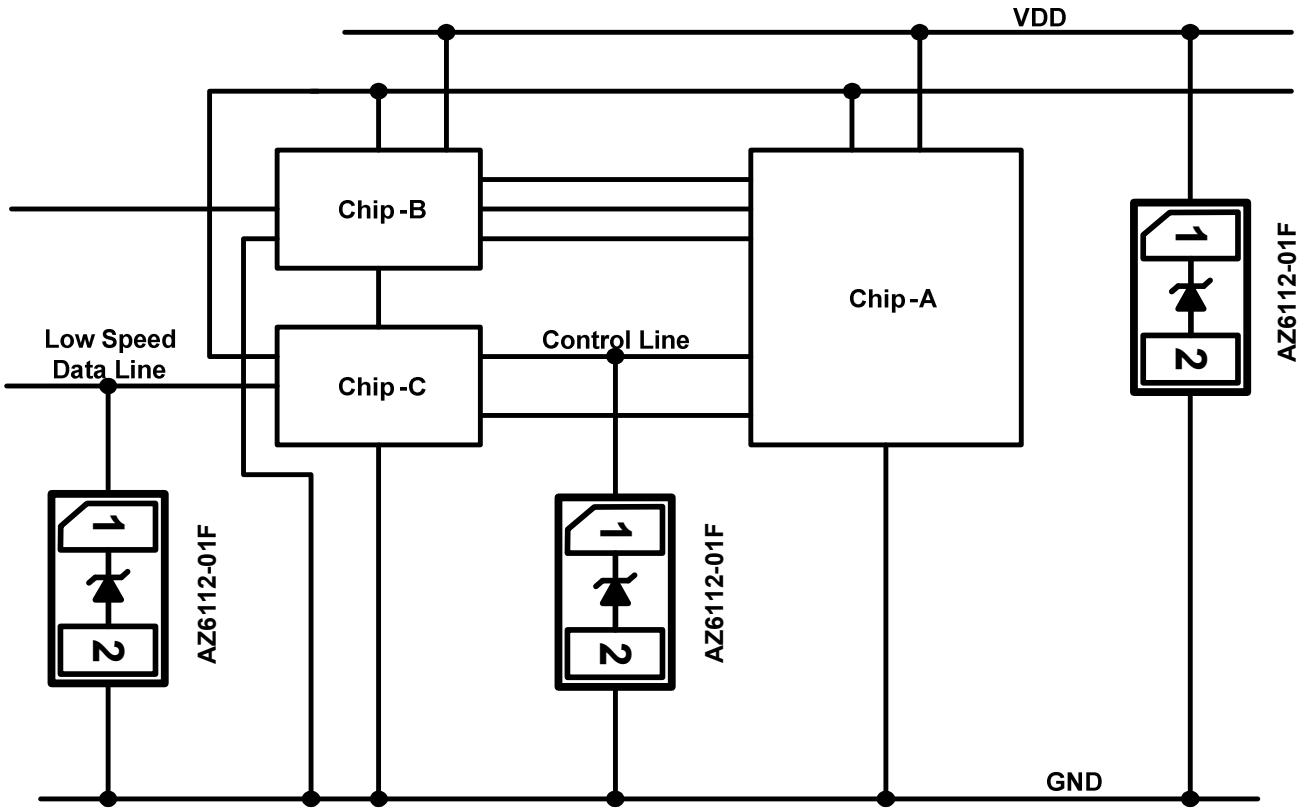
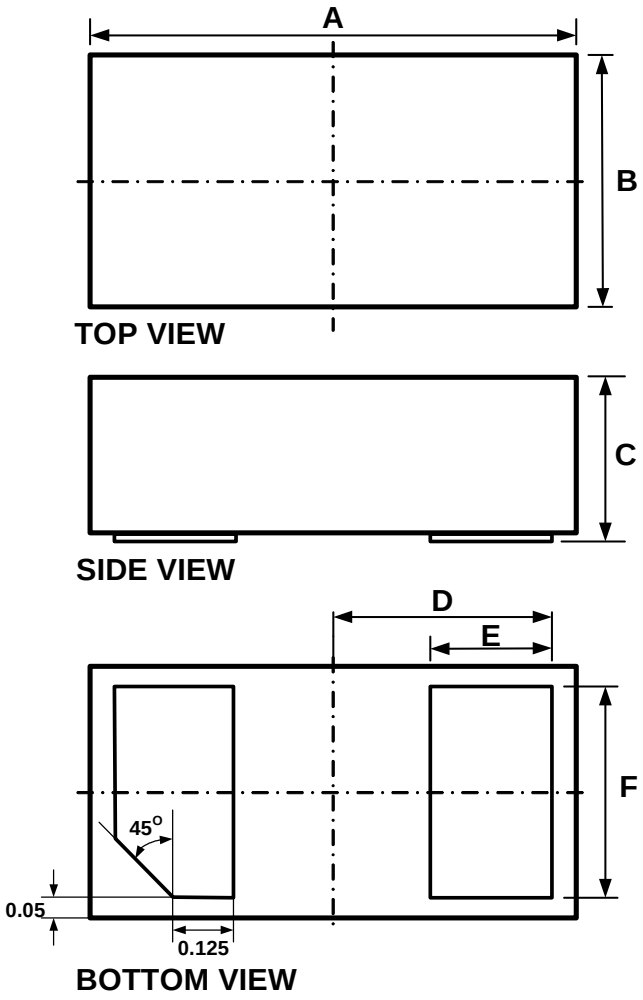


Fig. 2

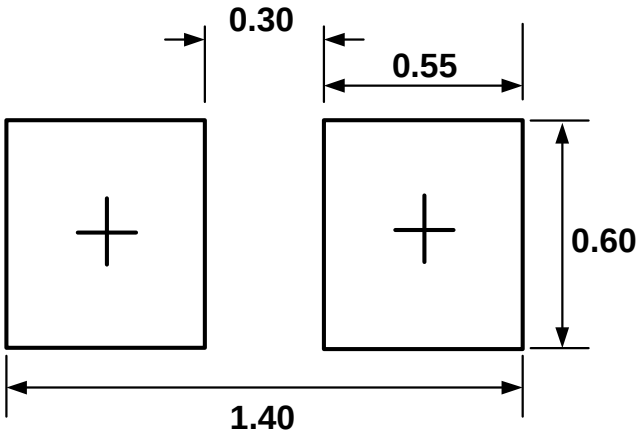
Mechanical Details

DFN1006P2E
PACKAGE DIAGRAMS



Symbol	Millimeters		Inches	
	min	max	min	max
A	0.95	1.05	0.037	0.041
B	0.55	0.65	0.022	0.026
C	0.45	0.60	0.018	0.024
D	0.45 BSC		0.018 BSC	
E	0.20	0.30	0.008	0.012
F	0.45	0.55	0.018	0.022

LAND LAYOUT

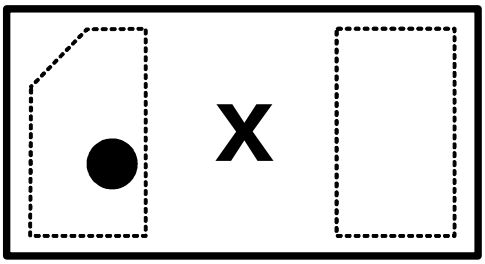


(Unit: mm)

Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



Top View

Part Number	Marking Code
AZ6112-01F (Green Part)	x

Note : Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ6112-01F.R7GR	Green	T/R	7 inch	12,000/reel	4 reel=48,000/box	6 box=288,000/carton

Revision History

Revision	Modification Description
Revision 2014/04/25	Preliminary Release.
Revision 2014/12/22	Update the Ordering Information.
Revision 2015/04/28	Formal Release.