Features

- ESD protection for two lines with bi-directional
- Provide transient protection for each line to
  IEC 61000-4-2 (ESD) ±30kV (air / contact)
  IEC 61000-4-4 (EFT) 80A (5/50ns)
  IEC 61000-4-5 (Lightning) 20A (8/20μs)
- Suitable for, **6V and below**, operating voltage applications
- Fast turn-on and low clamping voltage
- Array of ESD rated equivalent TVS diodes
- Small package saves board space
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

- Power supply protection
- Data and I/O lines protection
- Panels
- Handheld portable application
- Portable devices
- Consumer electronics
- Notebooks, desktops, and servers
- Peripherals

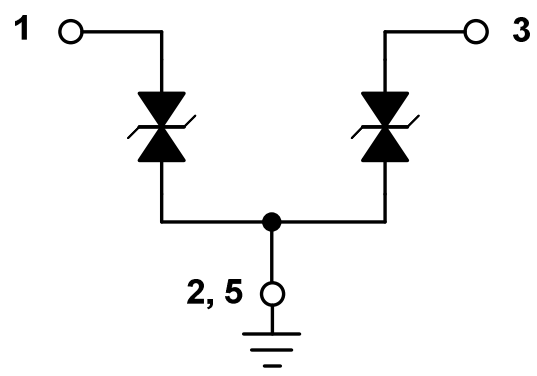
Description

AZ5926-02F is a design which includes two bi-directional ESD/surge rated clamping cell arrays to protect the power lines or control lines in an electronic system. The AZ5926-02F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

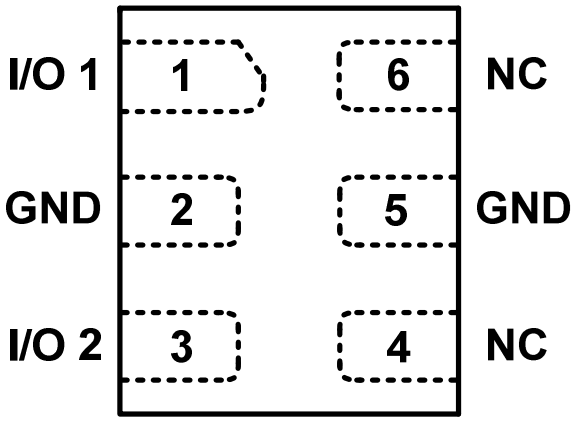
AZ5926-02F is a unique design which includes proprietary clamping cells in a single package. During transient conditions, the proprietary clamping cells prevent over-voltage on the power lines or control lines, protecting any downstream components.

AZ5926-02F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



DFN1210P6X (Top View)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A= 25°C, unless otherwise specified)			
PARAMETER	**SYMBOL**	**RATING**	**UNIT**
Peak Pulse Current (tp =8/20μs)	I_{PP} (Note 1)	20	A
Operating Voltage (I/O pin-GND)	V_{DC}	6.5	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD-1} V_{ESD-2}	±30 ±30	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +125	°C
Storage Temperature	T_{STO}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITION**	**MIN**	**TYP**	**MAX**	**UNIT**
Reverse Stand-Off Voltage	V_{RWM}	Pin-1,-3 to pin-2, -5, T=25 °C.	-6		6	V
Channel Leakage Current	$I_{CH-Leak}$	$V_{Pin-1,-3}$ = 6V, $V_{Pin-2,-5}$ = 0V, T=25 °C.			1	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, pin-1, -3 to pin-2, -5.	6.7		10	V
Surge Clamping Voltage (Note 1)	$V_{CL-surge}$	I_{PP}=5A, tp=8/20μs, T=25 °C, any I/O pin to GND.		10		V
		I_{PP}=20A, tp=8/20μs, T=25 °C, any I/O pin to GND.		13		V
ESD Clamping Voltage (Note 2)	V_{ESD_CL}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), Contact mode, T=25 °C, any I/O pin to GND.		10.5		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2, 0 ~ +8kV, Contact mode, T=25 °C, any I/O pin to GND.		0.14		Ω
Channel Input Capacitance	C_{IN}	$V_{Pin-2,-5}$ = 0V, V_{IN} = 0V, f = 1MHz, T=25 °C, any I/O pin to GND.		32	40	pF

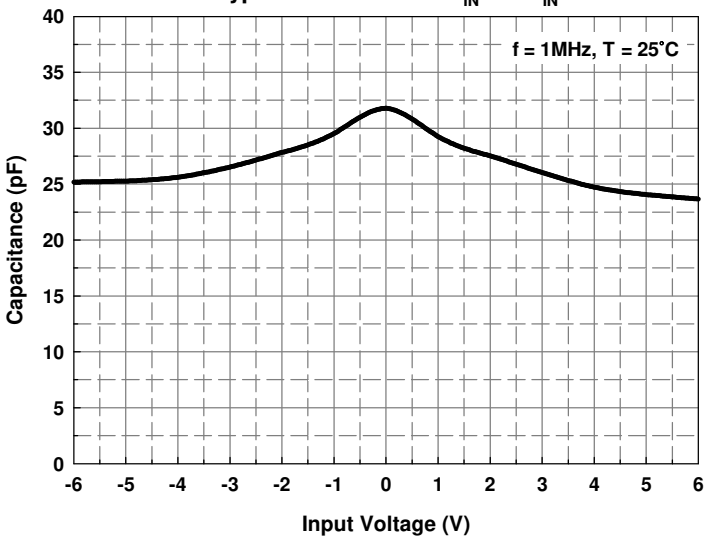
Note 1: The Peak Pulse Current measured conditions: t_p = 8/20μs, 2Ω source impedance.

Note 2: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

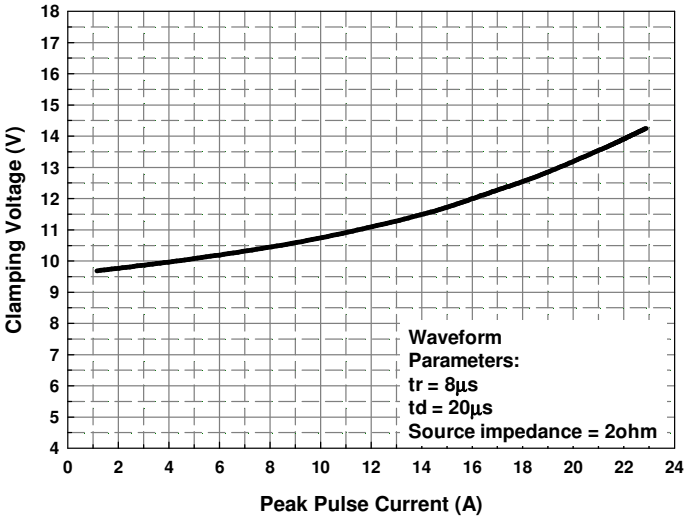
TLP conditions: Z_0 = 50Ω, t_p = 100ns, t_r = 1ns.

Typical Characteristics

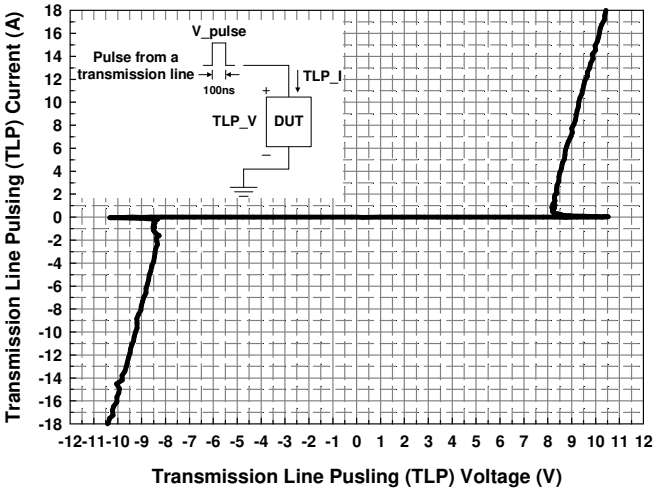
Typical Variation of C_{IN} vs. V_{IN}



Clamping Voltage vs. Peak Pulse Current



Transmission Line Pulsing (TLP) Measurement



Application Information

The AZ5926-02F is designed to protect two lines against system ESD/Lightning pulses by clamping them to an acceptable reference. It provides bi-directional protection.

The device connection of the AZ5926-02F is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin 1 and pin 3 respectively. **The pin2 and pin5 are the ground pins. These two pins should be directly connected to the GND rail of PCB (Printed Circuit Board).** In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ5926-02F should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ5926-02F.
- Place the AZ5926-02F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

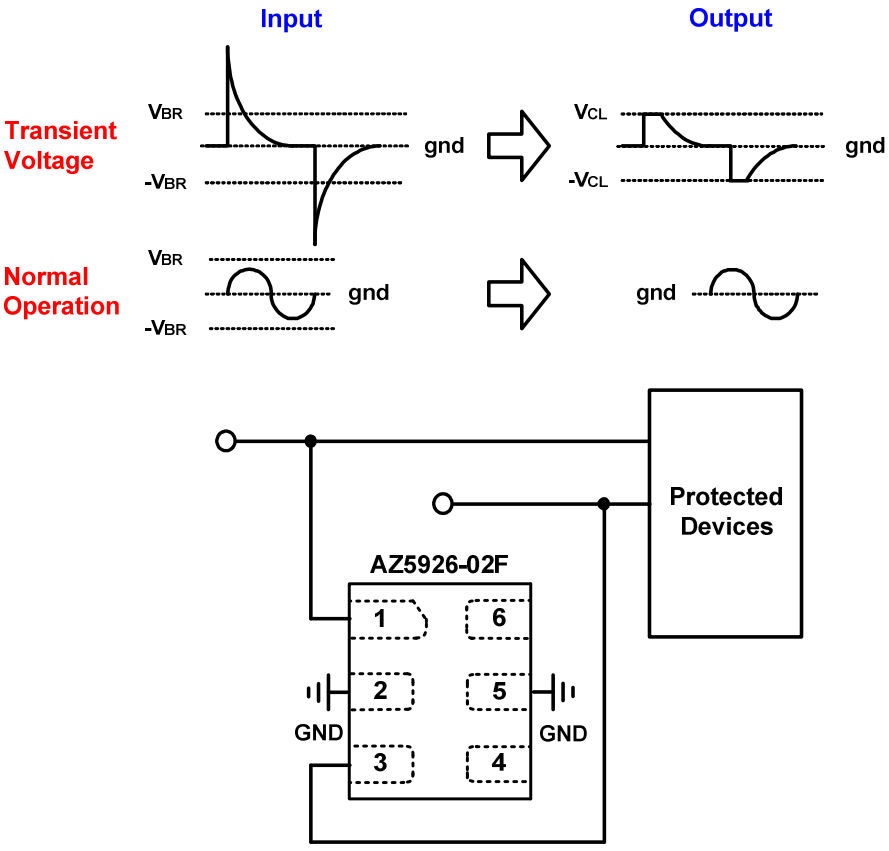


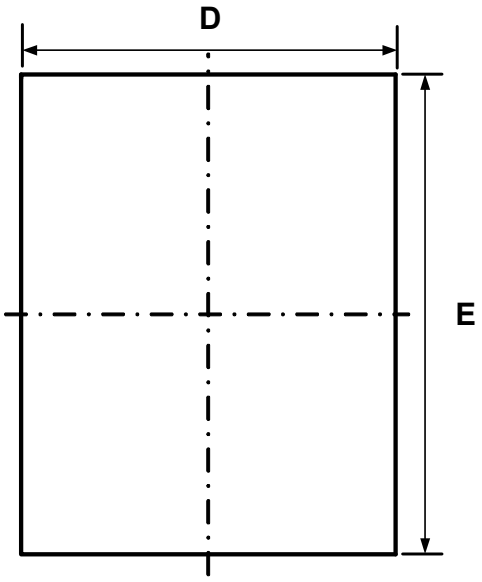
Fig. 1

Mechanical Details

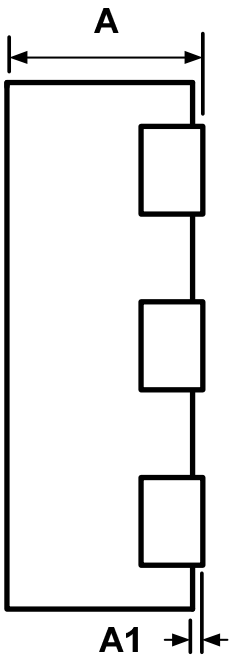
DFN1210P6X

PACKAGE DIAGRAMS AND DIMENSIONS

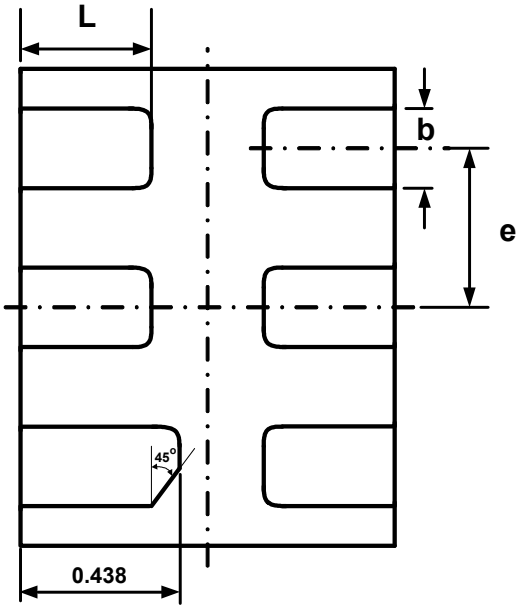
TOP VIEW



SIDE VIEW

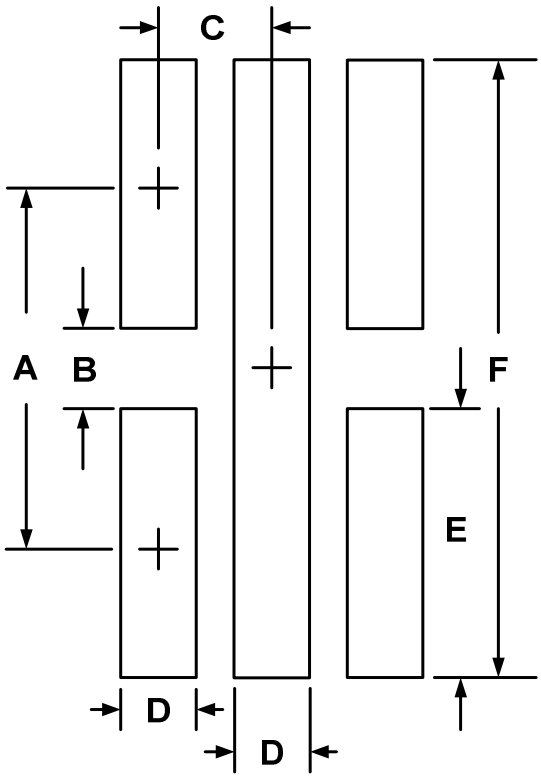


BOTTOM VIEW



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
D	0.95	1.00	1.05
E	1.15	1.20	1.25
A	0.41	0.45	0.50
A1	0.00	0.02	0.05
e		0.40 BSC	
b	0.15	0.20	0.25
L	0.25	0.35	0.45

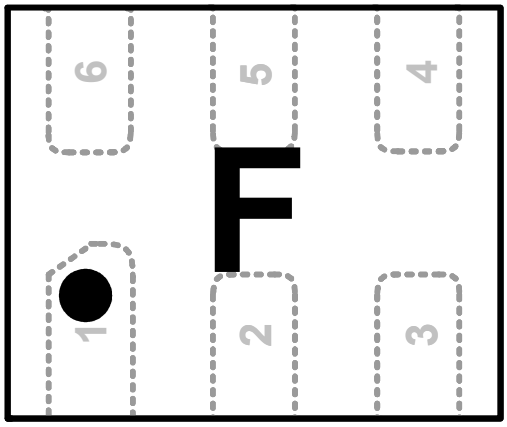
LAND LAYOUT



Dimensions		
Index	Millimeter	Inches
A	0.875	0.034
B	0.20	0.008
C	0.40	0.016
D	0.20	0.008
E	0.675	0.027
F	1.55	0.061

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



Part Number	Marking Code
AZ5926-02F.R7G (Green Part)	F

Note : Green means Pb-free, RoHS, and Halogen free compliant.

F = Device Code

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ5926-02F.R7G	Green	T/R	7 inch	3,000/reel	4 reels = 12,000/box	6 boxes =72,000/carton

Revision History

Revision	Modification Description
Revision 2018/05/17	Formal Release.