Features

- ESD protect for one line with bi-directional
- Provide transient protection for the protected line to

  IEC 61000-4-2 (ESD) ±30kV (air), ±30kV (contact)

  IEC 61000-4-4 (EFT) 80A (5/50ns)

  IEC 61000-4-5 (Lightning) 55A (8/20μs)
- **0402 small DFN package** saves board space
- Protect one I/O line or one power line
- Fast turn-on and low clamping voltage
- For low operating voltage applications: 4.5V
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

- Audio protection
- Vbat pin for mobile device
- Power line protection
- Mobile phones
- Control signal line protection
- Hand held portable applications

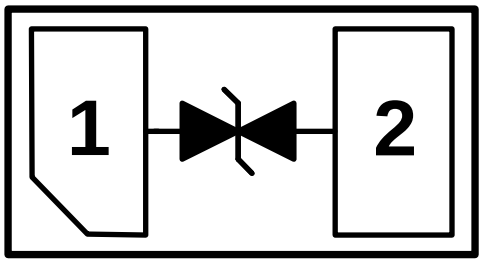
Description

AZ5845-01F is a design which includes a bi-directional surge rated clamping cell to protect one power line, or one control line, or one low-speed data line in an electronic system. The AZ5845-01F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ5845-01F is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ5845-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration



DFN1006P2X (Bottom View)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A= 25°C, unless otherwise specified)			
PARAMETER	**SYMBOL**	**RATING**	**UNIT**
Peak Pulse Current (tp =8/20μs)	I_{PP} (Note 1)	55	A
Operating Supply Voltage	V_{DC}	±4.6	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD-1} V_{ESD-2}	±30 ±30	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +125	°C
Storage Temperature	T_{STO}	-55 to +150	°C

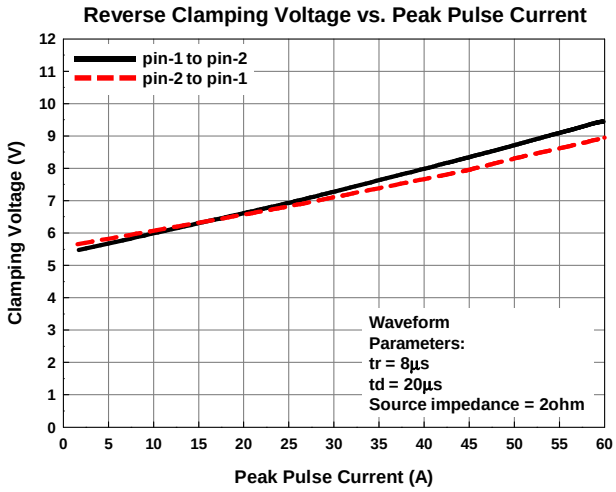
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITION**	**MIN**	**TYP**	**MAX**	**UNIT**
Reverse Stand-Off Voltage	V_{RWM}	T=25 °C.	-4.5		4.5	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = ±4.5V, T=25 °C.			100	nA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C.	4.7		8.0	V
Surge Clamping Voltage (Note 1)	$V_{CL-surge}$	I_{PP}=55A, tp=8/20μs, T=25 °C.		9	11	V
ESD Clamping Voltage (Note 2)	V_{CL-ESD}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), contact mode, T=25 °C.		6.5		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+8kV, contact mode, T=25 °C.		0.04		Ω
Channel Input Capacitance	C_{IN}	V_R = 0V, f = 1MHz, T=25 °C.		80	100	pF

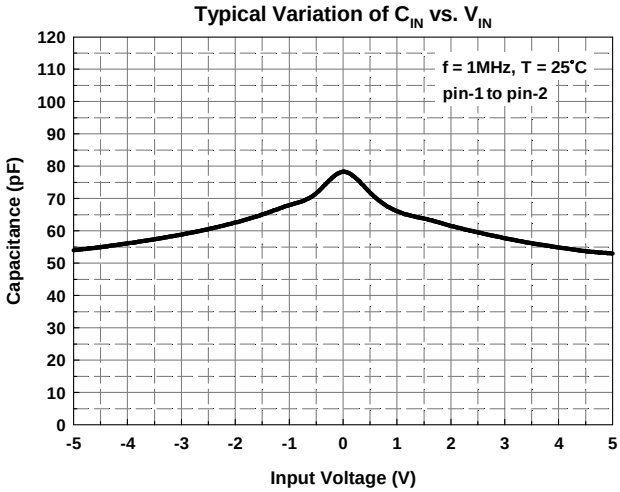
Note 1: The Peak Pulse Current measured conditions: t_p= 8/20μs, 2Ω source impedance.

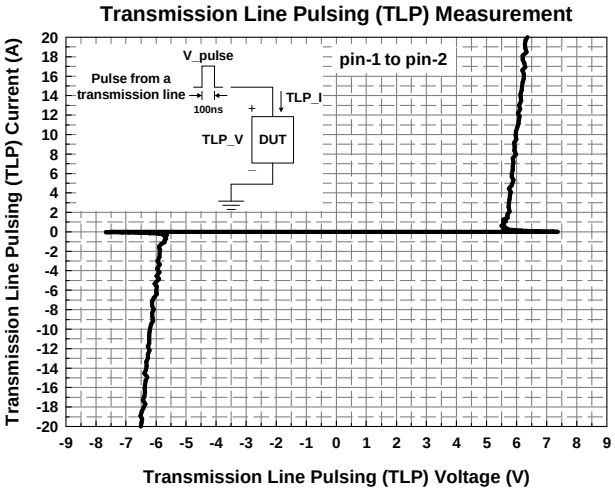
Note 2: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics







Application Information

The AZ5845-01F is designed to protect one line against system ESD/EFT/Lightning pulses by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ5845-01F is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ5845-01F should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ5845-01F.
- Place the AZ5845-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

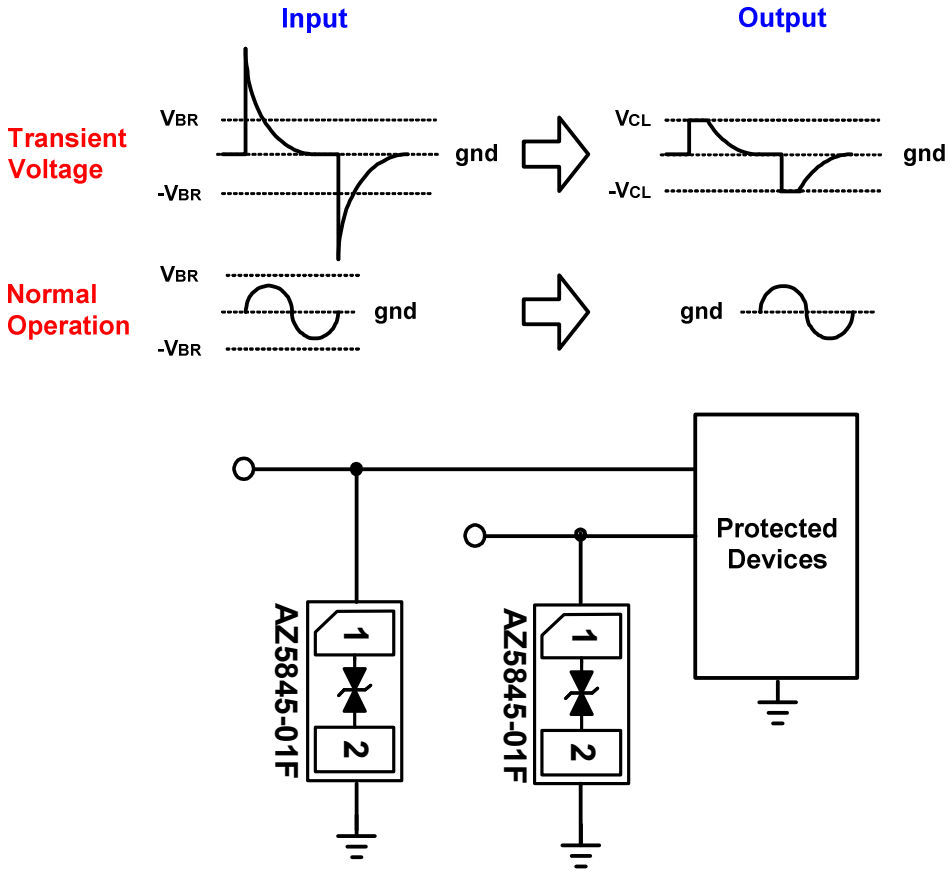


Fig. 1

Fig. 2 shows another simplified example of using AZ5845-01F to protect the control line, low-speed data line, and power line from ESD transient stress.

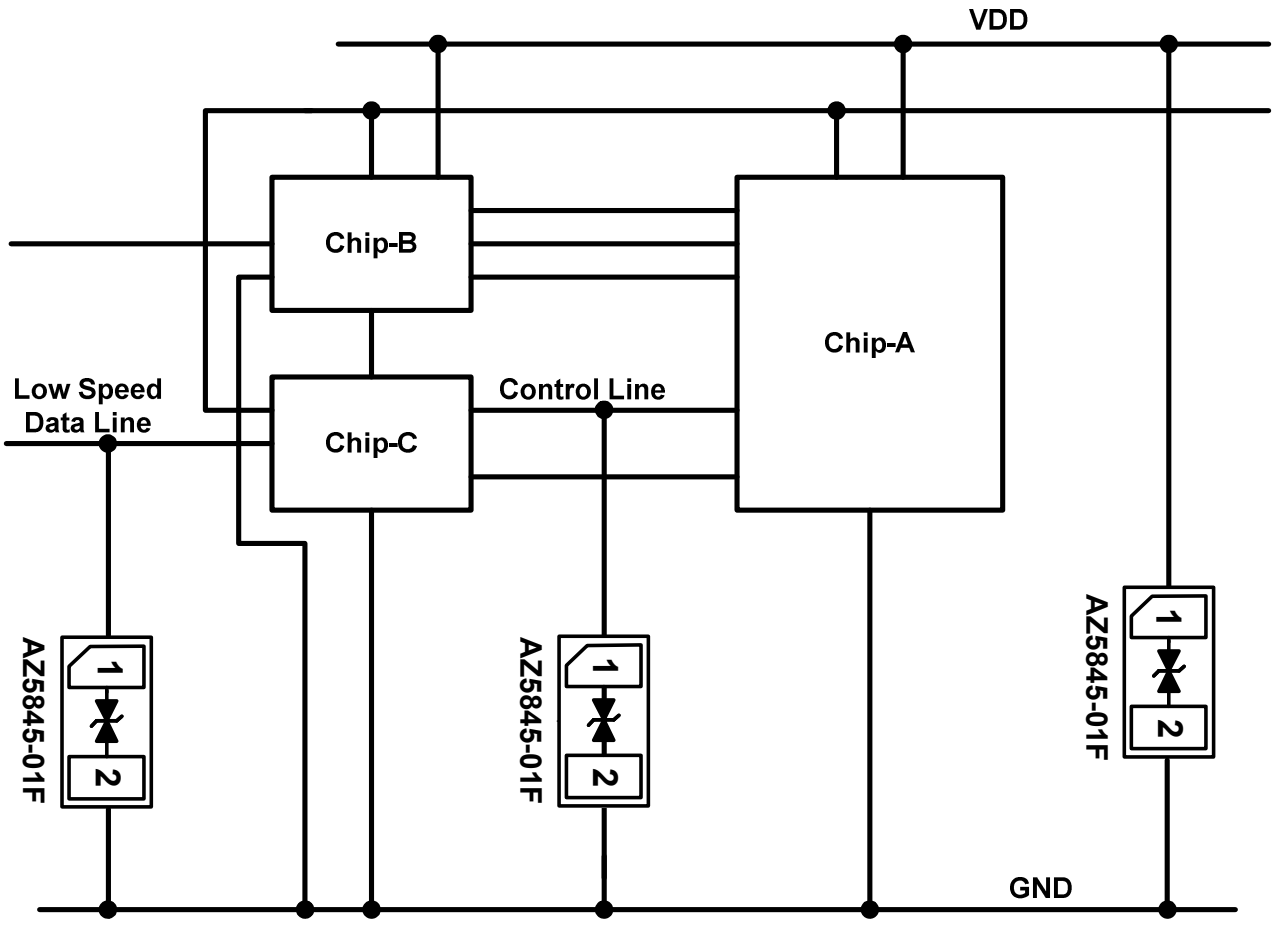
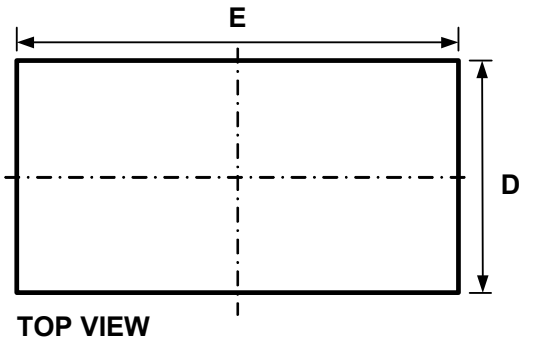


Fig. 2

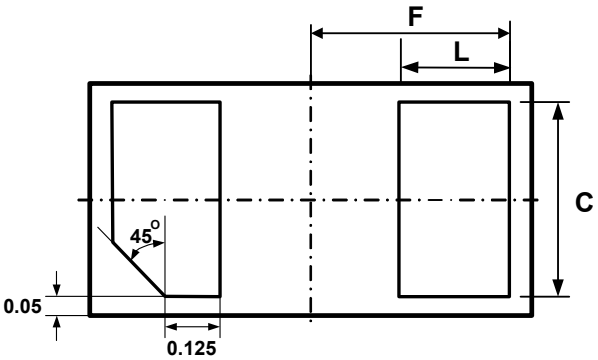
Mechanical Details

DFN1006P2X
PACKAGE DIAGRAMS



TOP VIEW

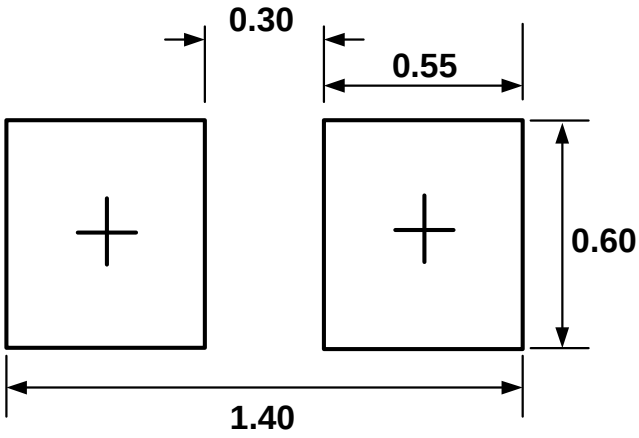
SIDE VIEW



BOTTOM VIEW

SYMBOL	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
E	0.95	1.05	0.037	0.041
D	0.55	0.65	0.022	0.026
A	0.40	0.55	0.016	0.022
F	0.45 BSC		0.018 BSC	
L	0.20	0.30	0.008	0.012
C	0.45	0.55	0.018	0.022

LAND LAYOUT

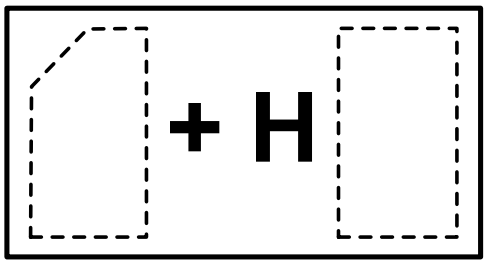


(Unit: mm)

Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



Top View

H=Device Code

Part Number	Marking Code
AZ5845-01F.R7GR (Green part)	H

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ5845-01F.R7GR	Green	T/R	7 inch	12,000/reel	4 reels = 48,000/box	6 boxes = 288,000/carton

Revision History

Revision	Modification Description
Revision 2019/05/03	Formal Release.