

## Features

- ESD/Surge Protection for 1 Line with Bidirectional.
- Provide transient protection for each line to  
IEC 61000-4-2 (ESD)  $\pm 30\text{kV}$  (air/contact)  
IEC 61000-4-4 (EFT) 80A (5/50ns)  
IEC 61000-4-5 (Lightning) 25A (8/20 $\mu\text{s}$ )
- Suitable for, 12V and below, operating voltage applications
- Small package saves board space
- Protect one I/O line or one power line
- Fast turn-on and Low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green part**

## Applications

- RS232, RS485 Interfaces
- Power line protection
- Security system
- Network
- Power manager system
- Notebooks, desktops, and servers
- Microprocessor-based equipment
- Peripherals

## Description

AZ4212-01G is a design which includes a bidirectional ESD rated clamping cell to protect one power line, or one control line, or one low speed data line in an electronic systems. The AZ4212-01G has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by

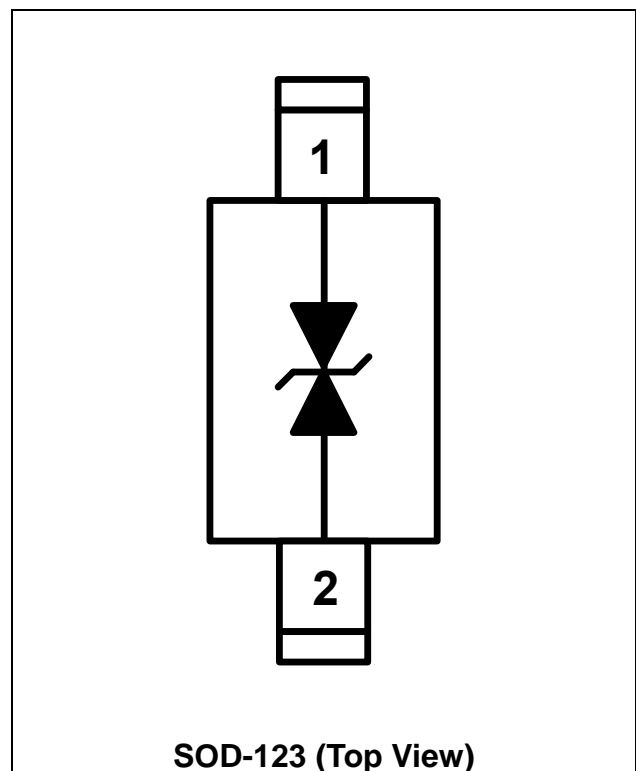
Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ4212-01G is a unique design which includes proprietary clamping cell in a single package.

During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ4212-01G may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ( $\pm 15\text{kV}$  air,  $\pm 8\text{kV}$  contact discharge).

## Circuit Diagram / Pin Configuration





## SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	SYMBOL	RATING	UNITS
Peak Pulse Current (tp =8/20μs)	I <sub>PP</sub>	25	A
Operating Supply Voltage	V <sub>DC</sub>	±13.2	V
ESD per IEC 61000-4-2 (Air)	V <sub>ESD-1</sub>	±30	kV
ESD per IEC 61000-4-2 (Contact)	V <sub>ESD-2</sub>	±30	
Lead Soldering Temperature	T <sub>SOL</sub>	260 (10 sec.)	°C
Operating Temperature	T <sub>OP</sub>	-55 to +85	°C
Storage Temperature	T <sub>STO</sub>	-55 to +150	°C

ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MINI	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V <sub>RVM</sub>	T=25 °C.	-12		12	V
Reverse Leakage Current	I <sub>Leak</sub>	V <sub>RVM</sub> = ±12V, T=25 °C			1	μA
Reverse Breakdown Voltage	V <sub>BV</sub>	I <sub>BV</sub> = 1mA, T=25 °C	13.7		18	V
Surge Clamping Voltage	V <sub>CL-surge</sub>	I <sub>PP</sub> =5A, tp=8/20μs, T=25 °C		16.5		V
		I <sub>PP</sub> =25A, tp=8/20μs, T=25 °C		21.5		V
ESD Clamping Voltage (Note 1)	V <sub>clamp</sub>	IEC 61000-4-2 +8kV (I <sub>TLP</sub> =16A), T=25 °C, Contact mode		17		V
ESD Dynamic Turn-on Resistance	R <sub>dynamic</sub>	IEC 61000-4-2 0~+8kV, T=25 °C, Contact mode		0.14		Ω
Channel Input Capacitance	C <sub>IN</sub>	V <sub>R</sub> =0V, f = 1MHz, T=25 °C		60	75	pF

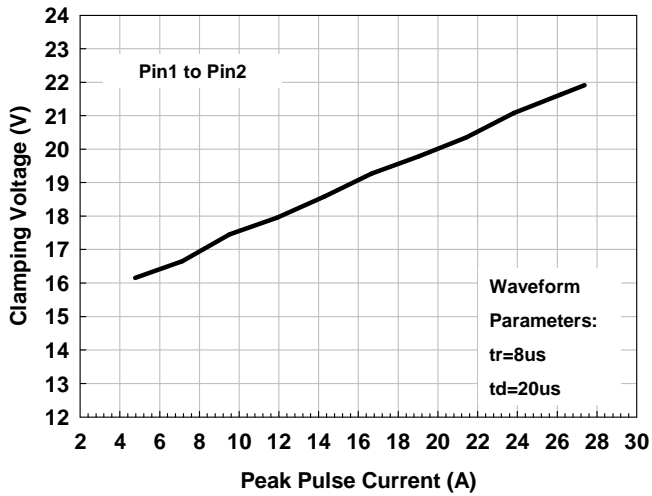
Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions: Z<sub>0</sub>= 50Ω, t<sub>p</sub>= 100ns, t<sub>r</sub>= 2ns.

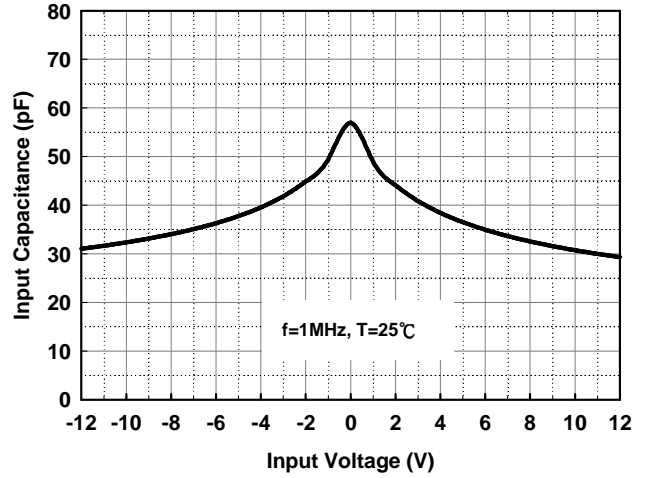


### Typical Characteristics

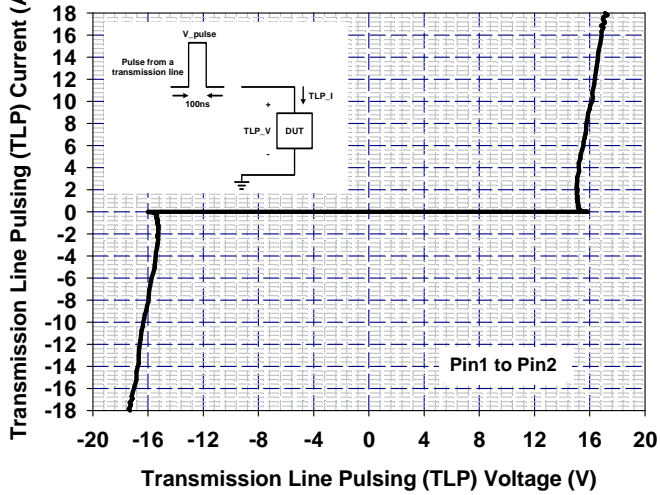
Reverse Clamping Voltage vs. Peak Pulse Current



Typical Variation of  $C_{IN}$  vs.  $V_{IN}$



Transmission Line Pulsing (TLP) Measurement



## Applications Information

The AZ4212-01G is designed to protect one line against System ESD/EFT/Lightning pulses by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ4212-01G is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ4212-01G should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ4212-01G.
- Place the AZ4212-01G near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

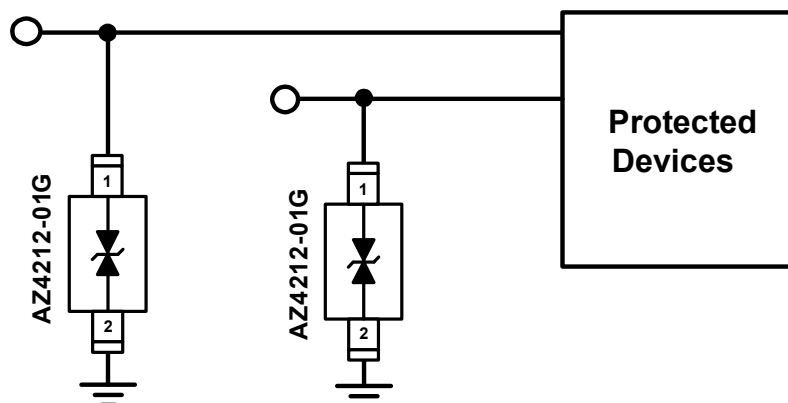
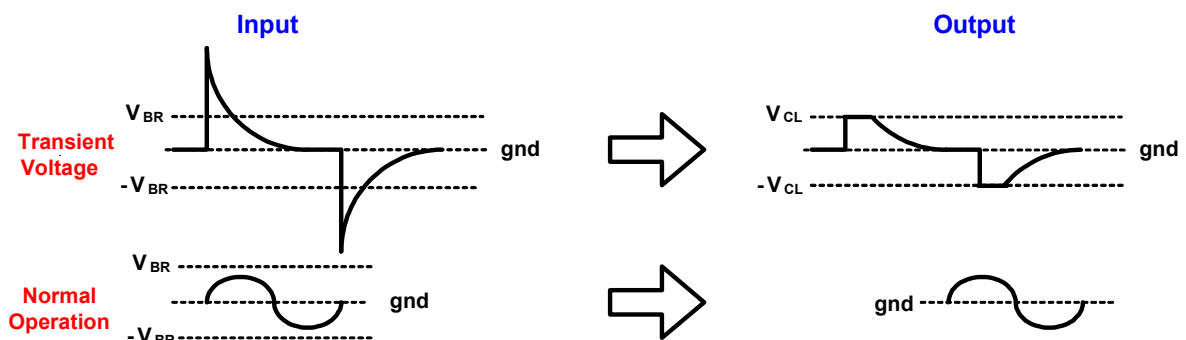


Fig. 1



Fig. 2 shows another simplified example of using AZ4212-01G to protect the control line, low speed data line, and power line from ESD transient stress.

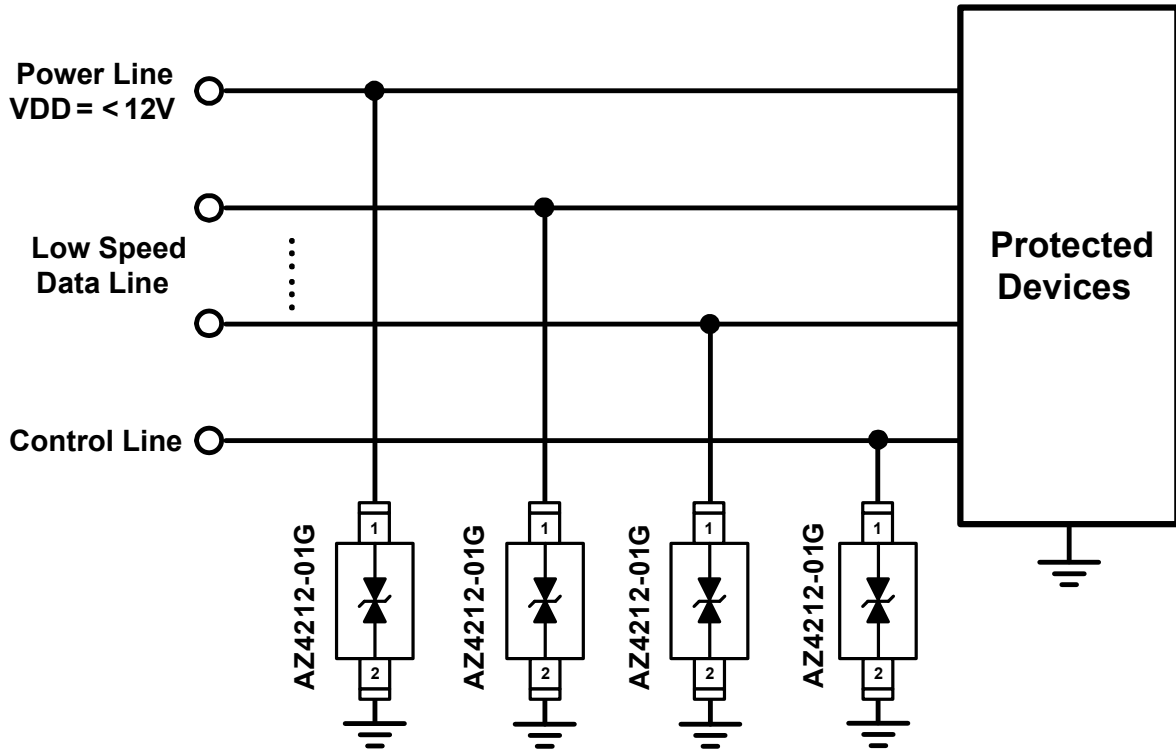
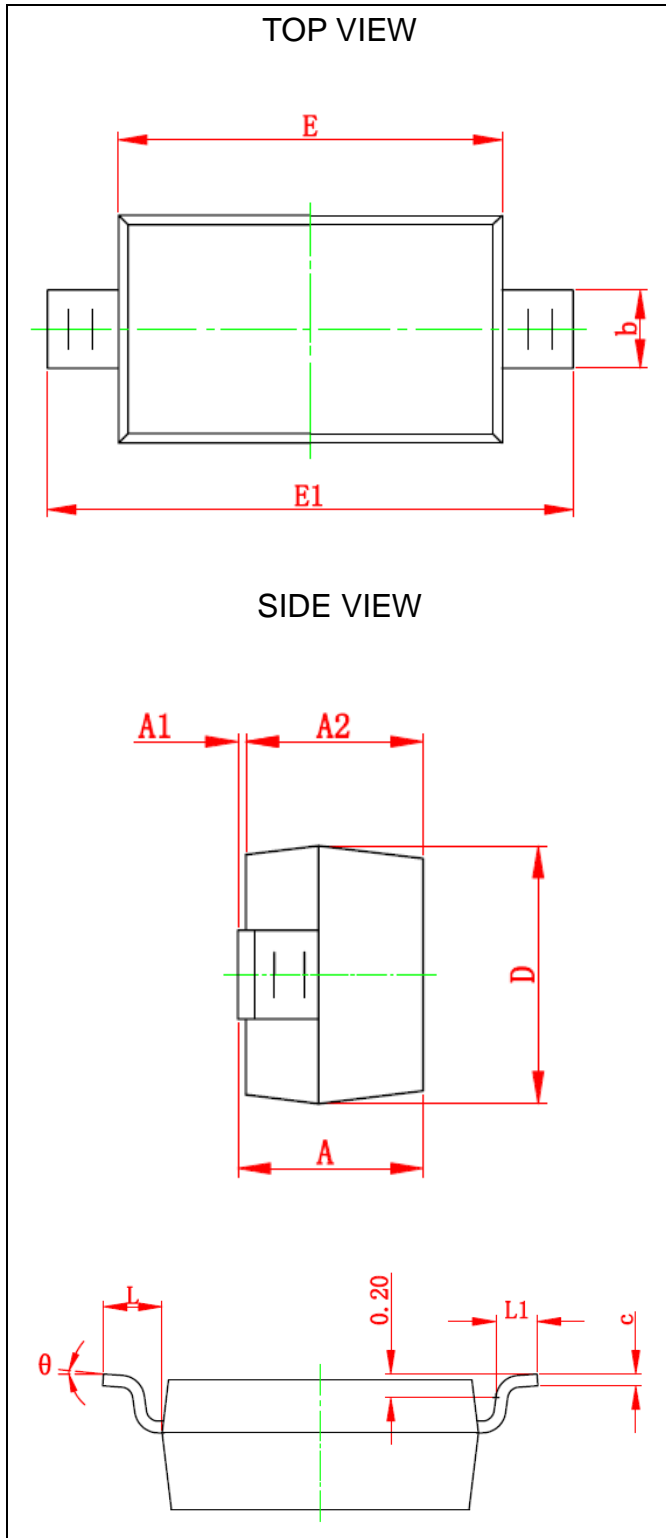


Fig. 2

## Mechanical Details

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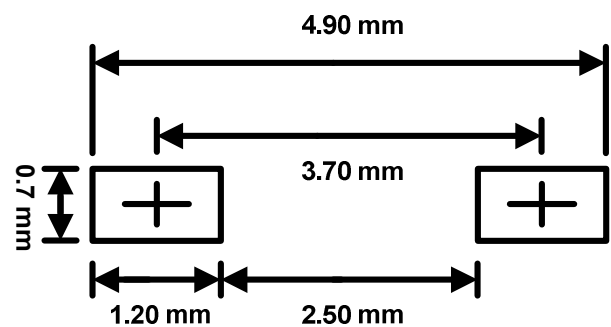
### PACKAGE DIAGRAMS



### PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	MIN.	MAX.	MIN.	MAX.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.450	0.650	0.018	0.026
c	0.080	0.150	0.003	0.006
D	1.500	1.700	0.059	0.067
E	2.600	2.800	0.102	0.110
E1	3.550	3.850	0.140	0.152
L	0.500 REF		0.020 REF	
L1	0.250	0.450	0.010	0.018
$\theta$	0°	8°	0°	8°

### LAND LAYOUT

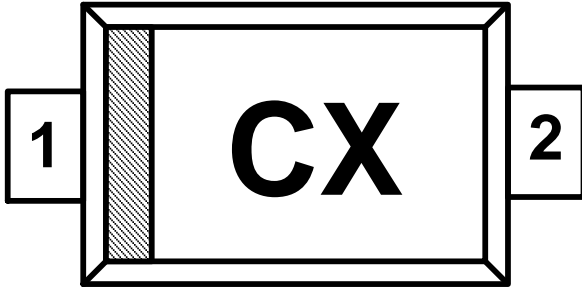


#### Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.



### MARKING CODE



C = Device Code  
X = Date Code

Part Number	Marking Code
AZ4212-01G (Green part)	CX

Note. Green means Pb-free, RoHS, and Halogen free compliant.

### Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ4212-01G.R7G	Green	T/R	7 inch	3,000/reel	4 reel= 12,000/box	6 box =72,000/carton

### Revision History

Revision	Modification Description
Revision 2014/11/27	Preliminary Release.
Revision 2015/03/26	Formal Release.