Features

- ESD/Surge protection for one line with uni-directional
- Provide transient protection for one line to
  IEC 61000-4-2 (ESD) ±30kV (air/contact)
  IEC 61000-4-4 (EFT) ±80A (5/50ns)
  IEC 61000-4-5 (Lightning) 13A (8/20μs)
- Suitable for**, 40V and below,** operating voltage applications
- Small package saves board space
- Protect one I/O line or one power line
- Fast turn-on and low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

- Battery contacts
- Power manager system
- Power line protection
- Portable devices
- Cellular handsets and accessories
- Notebooks, desktops, and servers
- Microprocessor-based equipment
- Peripherals

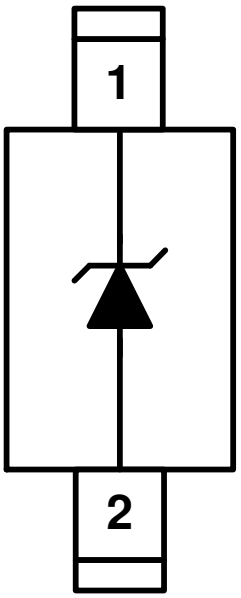
Description

AZ4040-01G is a design which includes a uni-directional ESD rated clamping cell to protect one power line, or one control line, or one low-speed data line in an electronic system. The AZ4040-01G has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT) , Lightning, and Cable Discharge Event (CDE).

AZ4040-01G is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ4040-01G may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration



SOD-123 (Top View)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A= 25°C, unless otherwise specified)			
PARAMETER	**SYMBOL**	**RATING**	**UNIT**
Peak Pulse Current (tp =8/20μs)	I_{PP}	13	A
Operating Supply Voltage (pin-1 to pin-2)	V_{DC}	44	V
Pin-1 to pin-2 ESD per IEC 61000-4-2 (Air) Pin-1 to pin-2 ESD per IEC 61000-4-2 (Contact)	V_{ESD-1} V_{ESD-2}	±30 ±30	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +85	°C
Storage Temperature	T_{STO}	-55 to +150	°C

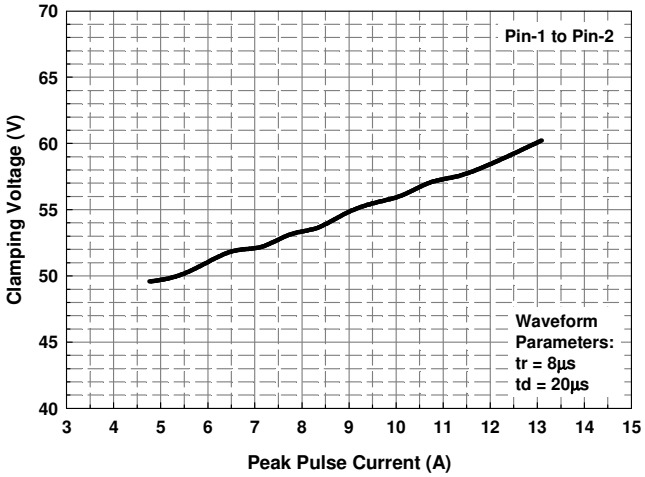
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITION**	**MIN**	**TYP**	**MAX**	**UNIT**
Reverse Stand-Off Voltage	V_{RWM}	Pin-1 to pin-2, T = 25°C.			40	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = 40V, T = 25°C, pin-1 to pin-2.			1	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T = 25°C, pin-1 to pin-2.	44.2			V
Forward Voltage	V_F	I_F = 15mA, T = 25°C, pin-2 to pin-1.	0.6		1.2	V
Surge Clamping Voltage	$V_{CL-surge}$	I_{PP} = 5A, tp = 8/20μs, T = 25°C, pin-1 to pin-2.		50		V
ESD Clamping Voltage (Note 1)	V_{CL-ESD}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), Contact mode, T = 25°C, pin-1 to pin-2.		53		V
Channel Input Capacitance	C_{IN}	V_R = 0V, f = 1MHz, T=25°C, pin-1 to pin-2.		200	300	pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

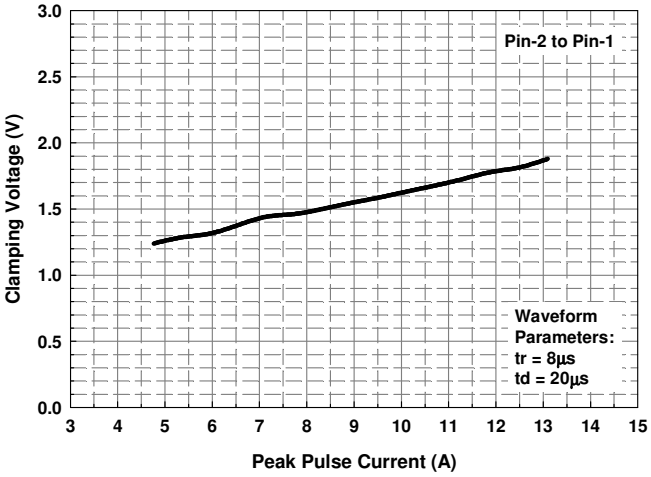
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics

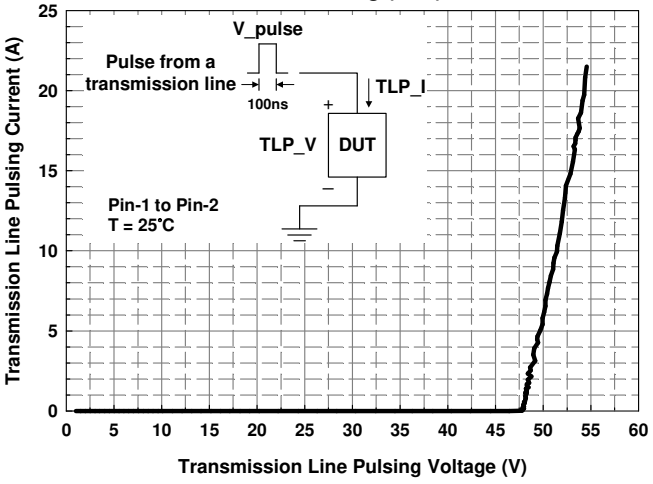
Reverse Clamping Voltage vs. Peak Pulse Current



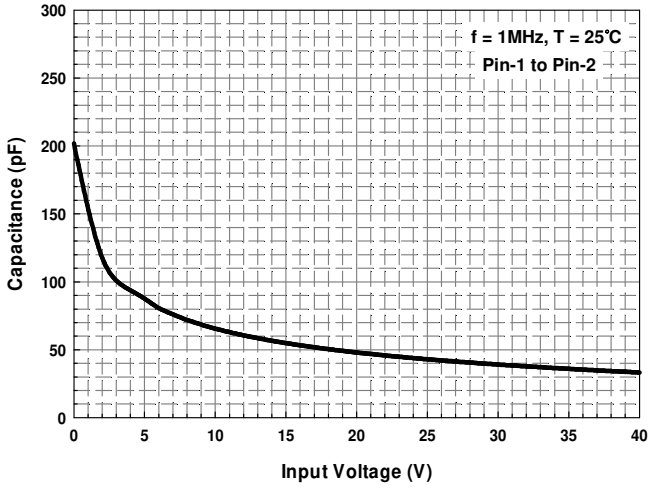
Forward Clamping Voltage vs. Peak Pulse Current



Transmission Line Pulsing (TLP) Measurement



Typical Variation of C_{IN} vs. V_{IN}



Application Information

The AZ4040-01G is designed to protect one line against system ESD/Lightning pulses by clamping them to an acceptable reference.

The usage of the AZ4040-01G is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin 1. The pin 2 should be connected directly to a ground plane on the board. All path lengths connected to the pins of AZ4040-01G should be kept as short as possible to minimize parasitic inductance in the board traces.

In order to obtain enough suppression of ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ4040-01G.
- Place the AZ4040-01G near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

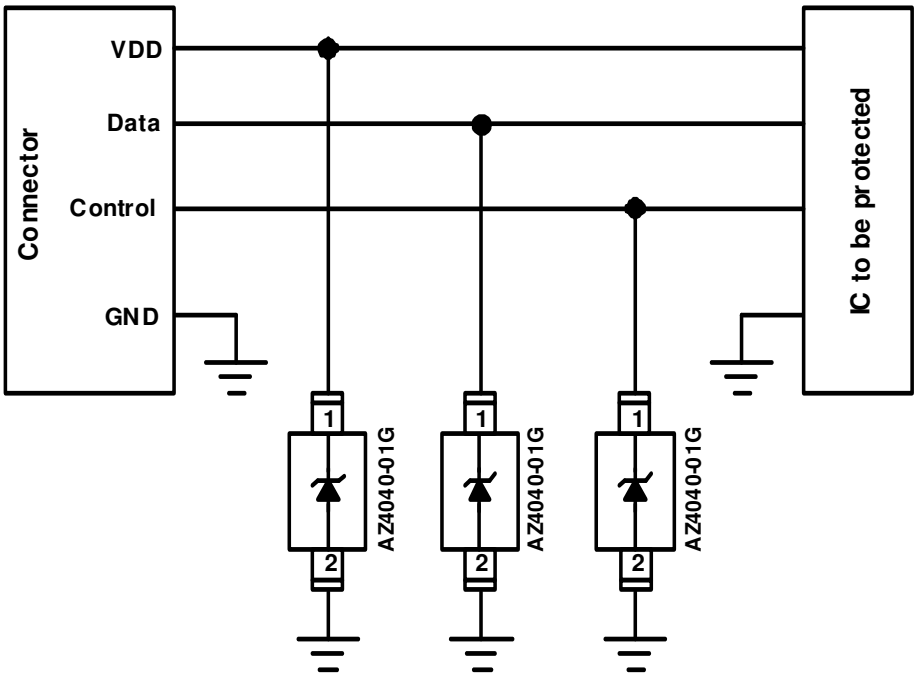


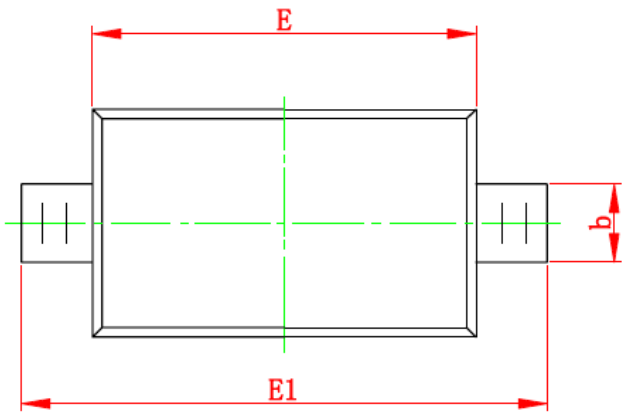
Fig. 1 ESD protection scheme by using AZ4040-01G

Mechanical Details

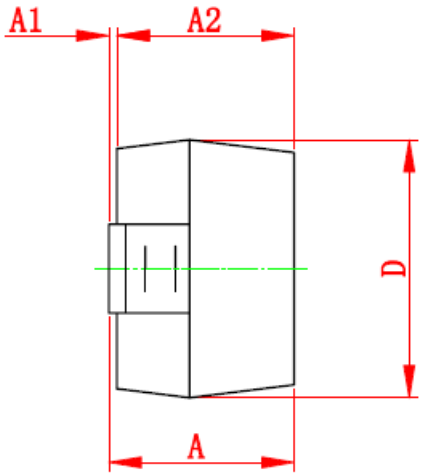
SOD-123

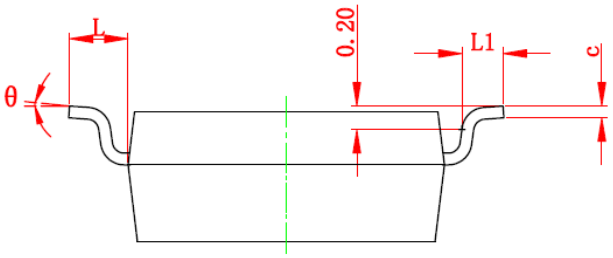
PACKAGE DIAGRAMS

TOP VIEW



SIDE VIEW

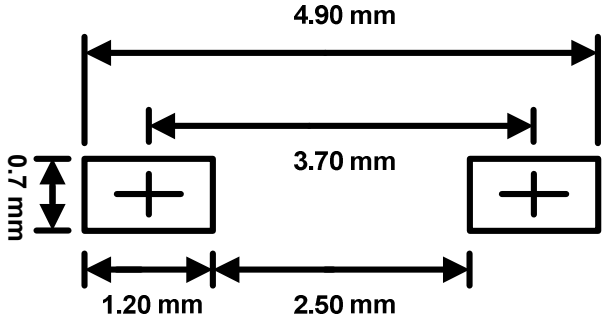




PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	MIN.	MAX.	MIN.	MAX.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.450	0.650	0.018	0.026
c	0.080	0.150	0.003	0.006
D	1.500	1.700	0.059	0.067
E	2.600	2.800	0.102	0.110
E1	3.550	3.850	0.140	0.152
L	0.500 REF		0.020 REF	
L1	0.250	0.450	0.010	0.018
θ	0°	8°	0°	8°

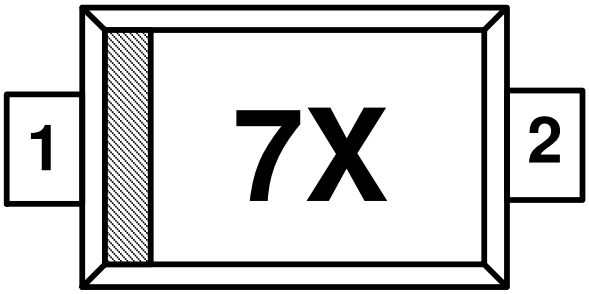
LAND LAYOUT



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



7 = Device Code
X = Date Code

Part Number	Marking Code
AZ4040-01G.R7G (Green Part)	7X

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ4040-01G.R7G	Green	T/R	7 inch	3,000/reel	4 reels = 12,000/box	6 boxes = 72,000/carton

Revision History

Revision	Modification Description
Revision 2016/01/15	Preliminary Release.
Revision 2018/03/19	Formal Release.