

Features

- ESD protection for one line with uni-direction
- Provide transient protection for the protected line to
 - IEC 61000-4-2 (ESD) $\pm 30\text{kV}$ (air/contact)
 - IEC 61000-4-4 (EFT) 80A (5/50ns)
 - IEC 61000-4-5 (Lightning) 25A (8/20 μs)
- Suitable for, **7.9V and below**, operating voltage applications
- **0402 small DFN package** saves board space
- Protect one I/O line or one power line
- Fast turn-on and low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green part**

Applications

- Power supply protection
- OLED
- Small panel modules
- Handheld portable applications
- Low speed data or control line protection
- Peripherals
- Consumer electronics

Description

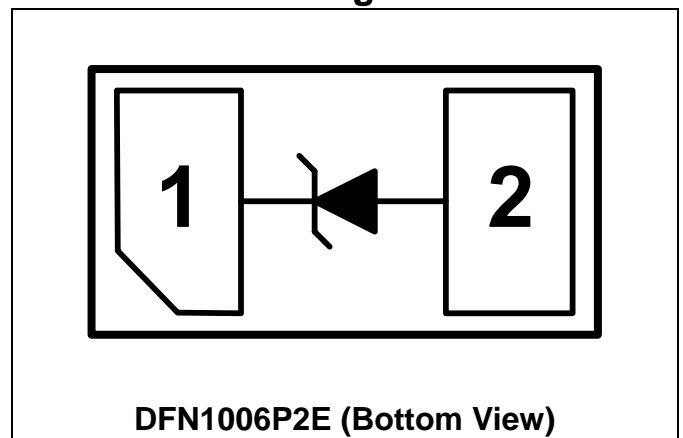
AZ4008-01F is a design which includes a uni-directional ESD rated clamping cell to protect one power line, one control line, or one low-speed data line in an electronic system. The AZ4008-01F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage caused by Electrostatic Discharging (ESD), Electrical Fast Transients

(EFT), Lightning, and Cable Discharge Event (CDE).

AZ4008-01F is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line, control line, or data line, protecting any downstream components.

AZ4008-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Circuit Diagram / Pin Configuration





SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$, unless otherwise specified)			
PARAMETER	SYMBOL	RATING	UNIT
Peak Pulse Current ($t_p=8/20\mu\text{s}$)	I_{PP}	25	A
Operating Voltage (pin-1 to pin-2)	V_{DC}	7.9	V
ESD per IEC 61000-4-2 (Air)	V_{ESD-1}	± 30	kV
ESD per IEC 61000-4-2 (Contact)	V_{ESD-2}	± 30	
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	$^\circ\text{C}$
Operating Temperature	T_{OP}	-55 to +125	$^\circ\text{C}$
Storage Temperature	T_{STO}	-55 to +150	$^\circ\text{C}$

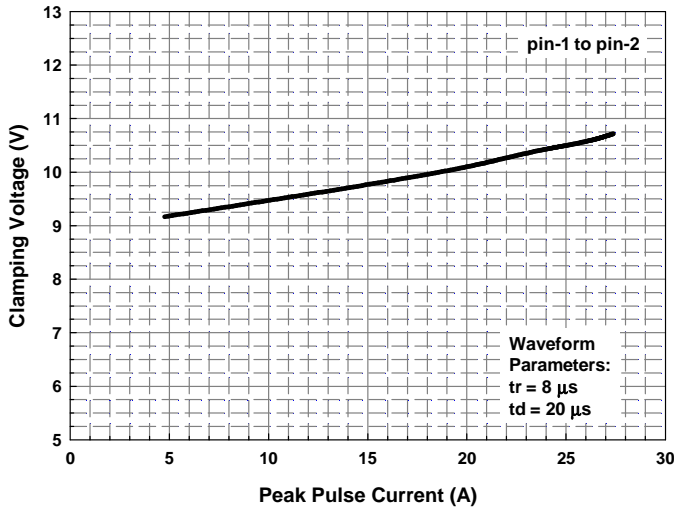
ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Reverse Stand-Off Voltage	V_{RWM}	Pin-1 to pin-2, $T = 25^\circ\text{C}$.			7.9	V
Reverse Leakage Current	I_{Leak}	$V_{RWM} = 7.9\text{V}$, $T = 25^\circ\text{C}$, pin-1 to pin-2.			250	nA
Reverse Breakdown Voltage	V_{BV}	$I_{BV} = 1\mu\text{A}$, $T = 25^\circ\text{C}$, pin-1 to pin-2.	8		9	V
Forward Voltage	V_F	$I_F = 15\text{mA}$, $T = 25^\circ\text{C}$, pin-2 to pin-1.	0.6		1.2	V
Surge Clamping Voltage	$V_{CL-surge}$	$I_{PP} = 10\text{A}$, $T = 25^\circ\text{C}$, pin-1 to pin-2.		9.5		V
		$I_{PP} = 25\text{A}$, $T = 25^\circ\text{C}$, pin-1 to pin-2.		10.5		V
ESD Clamping Voltage (Note 1)	V_{CL-ESD}	IEC 61000-4-2 +8kV ($I_{TLP} = 16\text{A}$), $T = 25^\circ\text{C}$, contact mode, pin-1 to pin-2.		10		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2, 0~+8kV, contact mode, $T = 25^\circ\text{C}$, pin-1 to pin-2.		0.05		Ω
Channel Input Capacitance	C_{IN}	$V_{IN} = 0\text{V}$, $f = 1\text{MHz}$, pin-1 to pin-2, $T = 25^\circ\text{C}$.		210	250	pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

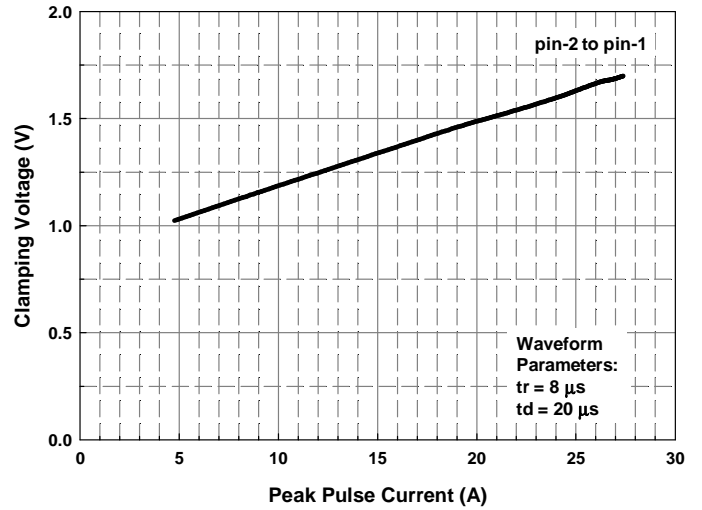
TLP conditions: $Z_0=50\Omega$, $t_p=100\text{ns}$, $t_r=1\text{ns}$.

Typical Characteristics

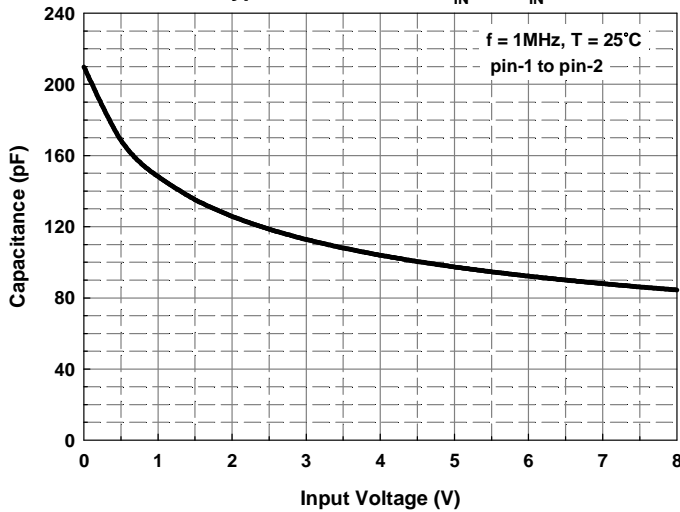
Reverse Clamping Voltage vs. Peak Pulse Current



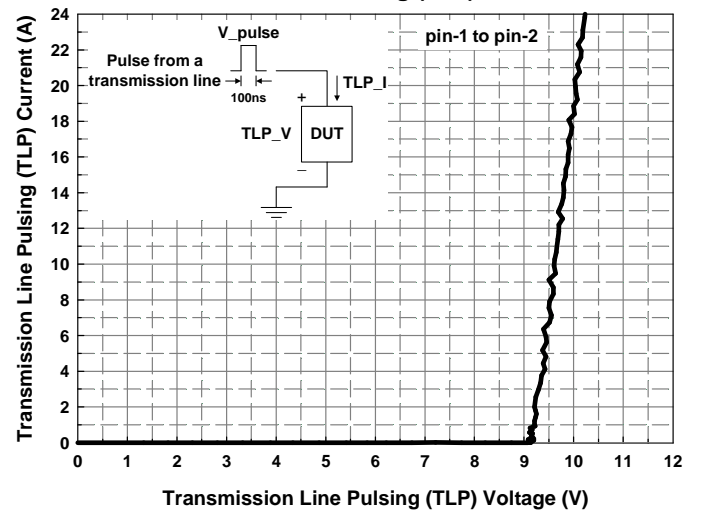
Forward Clamping Voltage vs. Peak Pulse Current



Typical Variation of C_{IN} vs. V_{IN}



Transmission Line Pulsing (TLP) Measurement



Application Information

The AZ4008-01F is designed to protect one line against system ESD / EFT / Lightning pulses by clamping it to an acceptable reference.

The usage of the AZ4008-01F is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected to pin 1. The pin 2 should be connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ4008-01F should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ4008-01F.
- Place the AZ4008-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

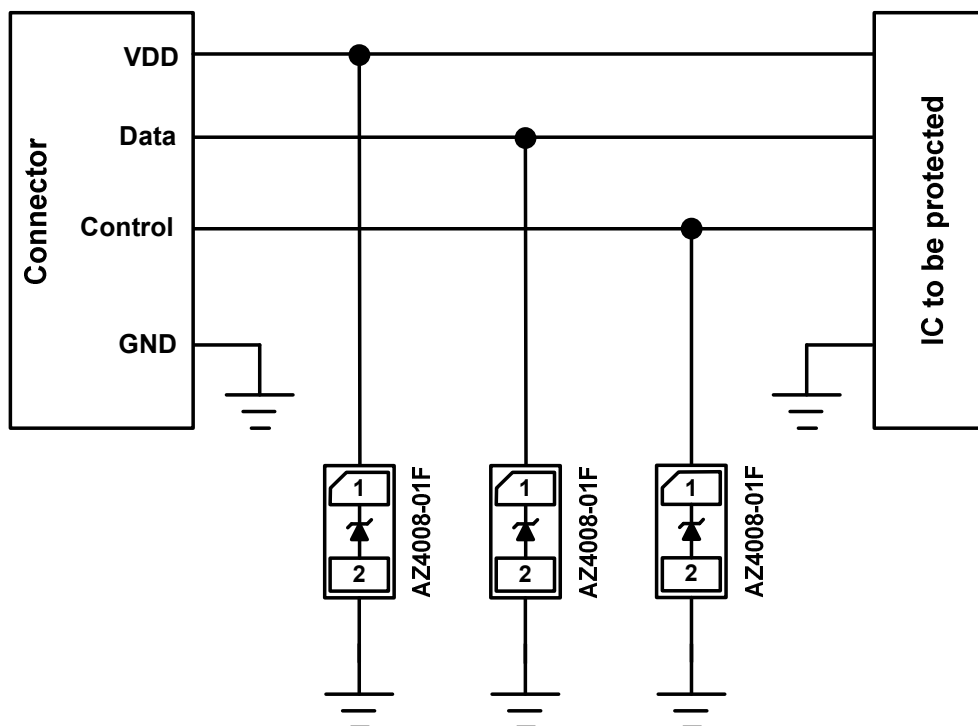
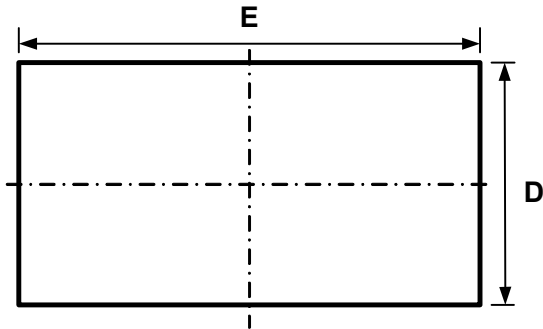


Fig. 1



Mechanical Details

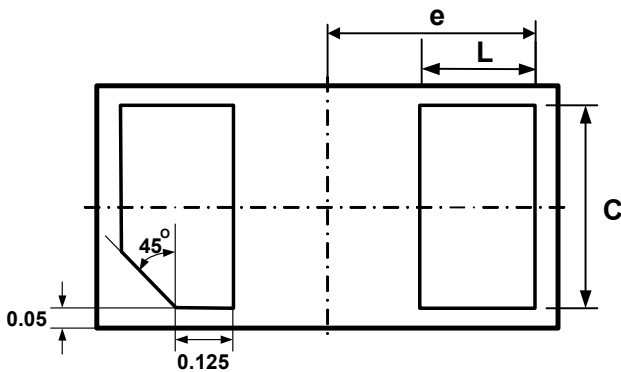
DFN1006P2E PACKAGE DIAGRAMS



TOP VIEW

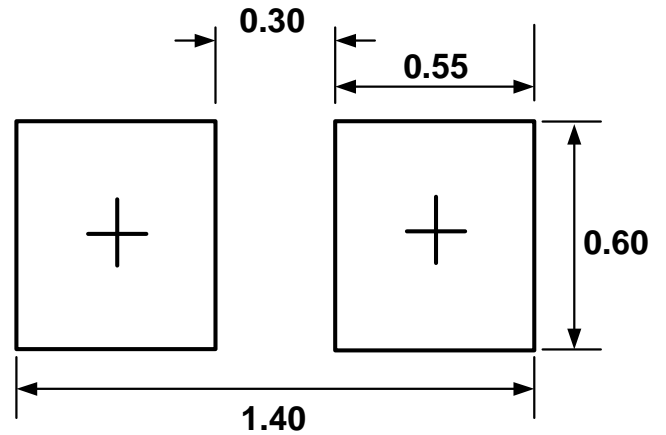


SIDE VIEW



BOTTOM VIEW

LAND LAYOUT



(Unit: mm)

Notes:

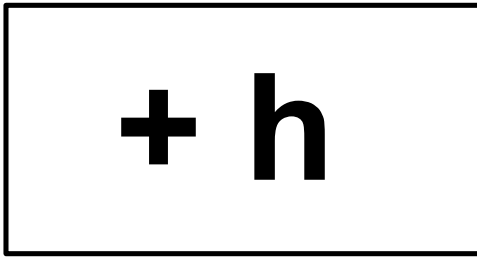
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

PACKAGE DIMENSIONS

SYMBOL	MILLIMETERS	
	MIN.	MAX.
E	0.95	1.05
D	0.55	0.65
A	0.45	0.55
e	0.45 BSC	
L	0.20	0.30
C	0.45	0.55



MARKING CODE



Top View

Part Number	Marking Code
AZ4008-01F.R7GR (Green Part)	h

Note. Green means Pb-free, RoHS, and Halogen free compliant.

h = Device Code

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ4008-01F.R7GR	Green	T/R	7 inch	12,000/reel	4 reels = 48,000/box	6 boxes = 288,000/carton

Revision History

Revision	Modification Description
Revision 2019/10/04	Formal Release.