

Features

- ESD/Surge protection for one line with uni-directional
- Provide transient protection for one line to **IEC 61000-4-2 (ESD) $\pm 30\text{kV}$ (air / contact)**
IEC 61000-4-4 (EFT) 80A (5/50ns)
IEC 61000-4-5 (Lightning) 200A (8/20 μs)
- For operating voltage of **4.5V and below**
- **1.6mm x 1.0mm DFN package** saves board space
- High surge protection
- Fast turn-on and low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green part**

Applications

- Vbat pin for mobile device
- Power line protection
- Mobile phones
- Hand held portable applications

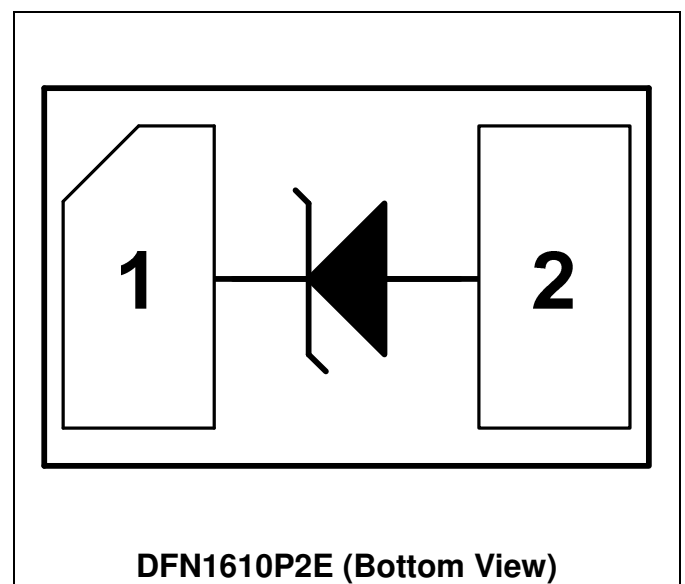
Description

AZ3505-01F is a design which includes a uni-directional surge rated clamping cell to protect one power line, or one control line, or one low-speed data line in an electronic system. The AZ3505-01F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ3505-01F is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ3505-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Circuit Diagram / Pin Configuration





SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C, unless otherwise specified)			
PARAMETER	SYMBOL	RATING	UNITS
Peak Pulse Current (tp=8/20μs)	I _{PP} (Note 1)	200	A
Operating Supply Voltage (pin-1 to pin-2)	V _{DC}	4.95	V
ESD per IEC 61000-4-2 (Air)	V _{ESD-1}	±30	kV
ESD per IEC 61000-4-2 (Contact)	V _{ESD-2}	±30	
Lead Soldering Temperature	T _{SOL}	260 (10 sec.)	°C
Operating Temperature	T _{OP}	-55 to +125	°C
Storage Temperature	T _{STO}	-55 to +150	°C

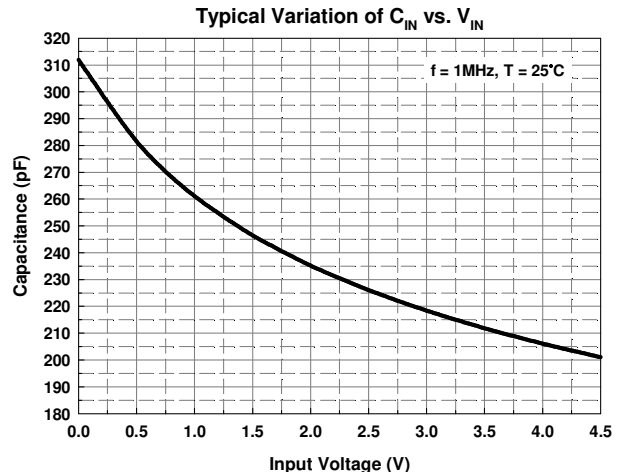
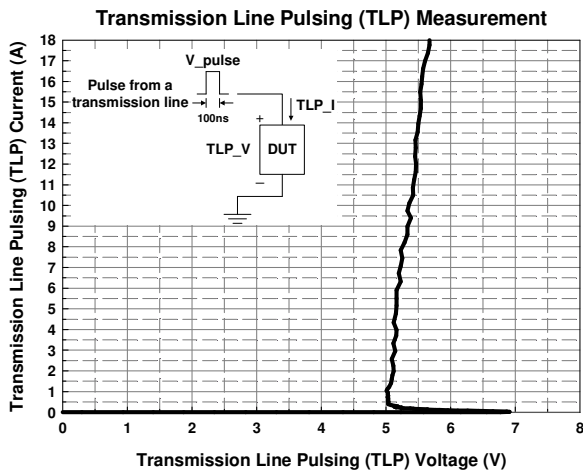
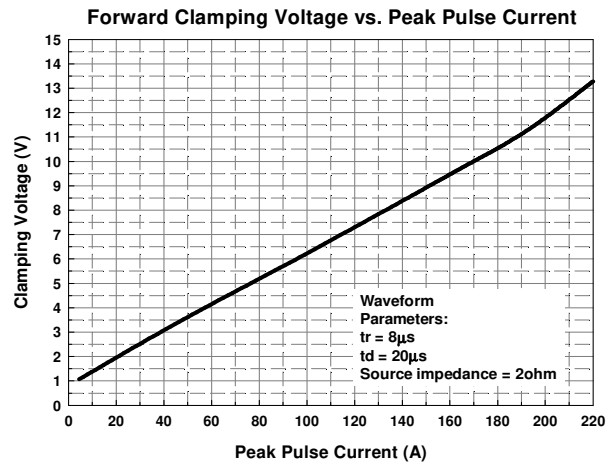
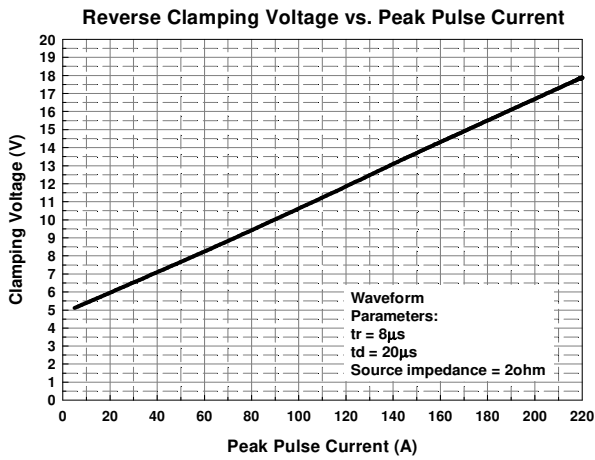
ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MINI	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V _{RWM}	Pin-1 to pin-2, T=25 °C.			4.5	V
Reverse Leakage Current	I _{Leak}	V _{RWM} = 4.5V, T=25 °C, pin-1 to pin-2.			100	nA
Reverse Breakdown Voltage	V _{BV}	I _{BV} = 1mA, T=25 °C, pin-1 to pin-2.	5		7	V
Forward Voltage	V _F	I _F = 15mA, T=25 °C, pin-2 to pin-1.		0.8	1	V
Surge Clamping Voltage (Note 1)	V _{CL-surge}	I _{PP} = 100A, tp=8/20μs, T=25 °C, pin-1 to pin-2.		10.5		V
		I _{PP} = 200A, tp=8/20μs, T=25 °C, pin-1 to pin-2.		16.5		
ESD Clamping Voltage (Note 2)	V _{CL-ESD}	IEC 61000-4-2 +8kV (I _{TLP} = 16A), Contact mode, T=25 °C, pin-1 to pin-2.		5.5		V
ESD Dynamic Turn-on Resistance	R _{dynamic}	IEC 61000-4-2 0~+8kV, Contact mode, T=25 °C, pin-1 to pin-2.		0.03		Ω
Channel Input Capacitance	C _{IN}	V _R = 0V, f = 1MHz, T=25 °C, pin-1 to pin-2.		310	400	pF

Note 1: The Peak Pulse Current measured conditions: t_p= 8/20μs, 2Ω source impedance.

Note 2: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions: Z₀= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics



Applications

The AZ3505-01F is designed to protect one line against system ESD/EFT/Lightning pulses by clamping them to an acceptable reference.

The usage of the AZ3505-01F is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected to pin 1. The pin 2 should be connected directly to a ground plane on the board. All path lengths connected to the pins of AZ3505-01F should be kept as short as possible to minimize parasitic inductance in the board traces.

In order to obtain enough suppression of ESD induced transient, a good circuit board is critical.

Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ3505-01F.
- Place the AZ3505-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

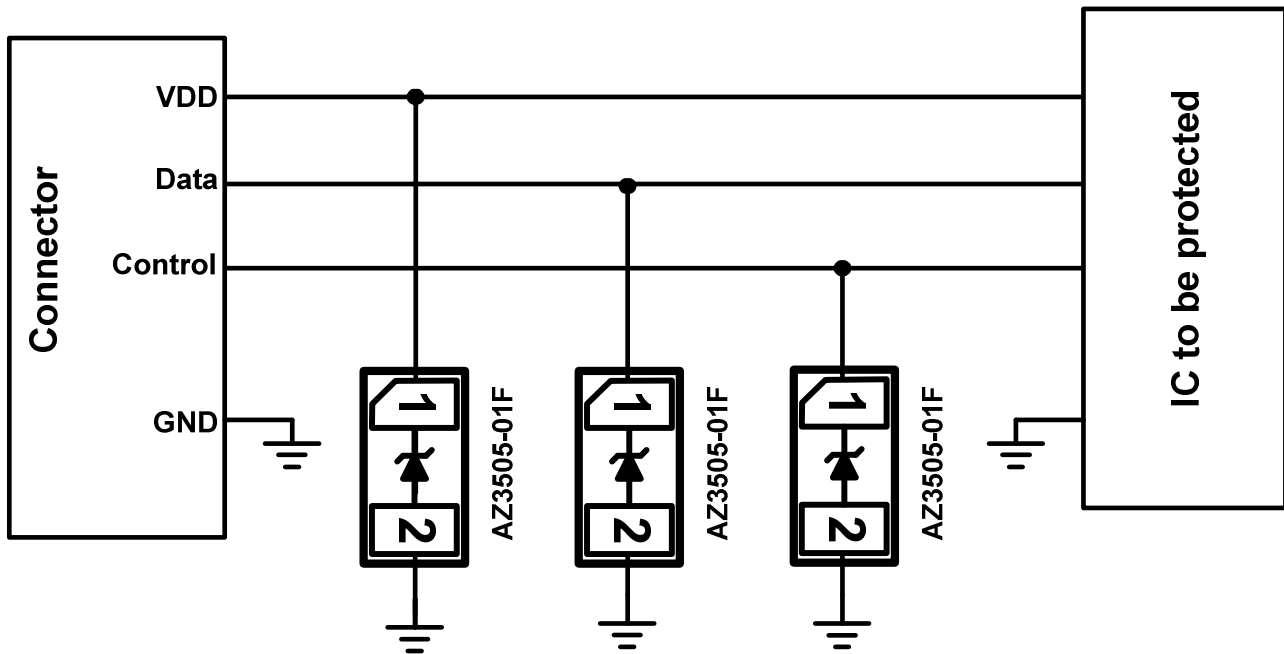


Fig. 1

Fig. 2 shows another simplified example of using AZ3505-01F to protect the control lines, low-speed data lines, and power lines from ESD transient stress.

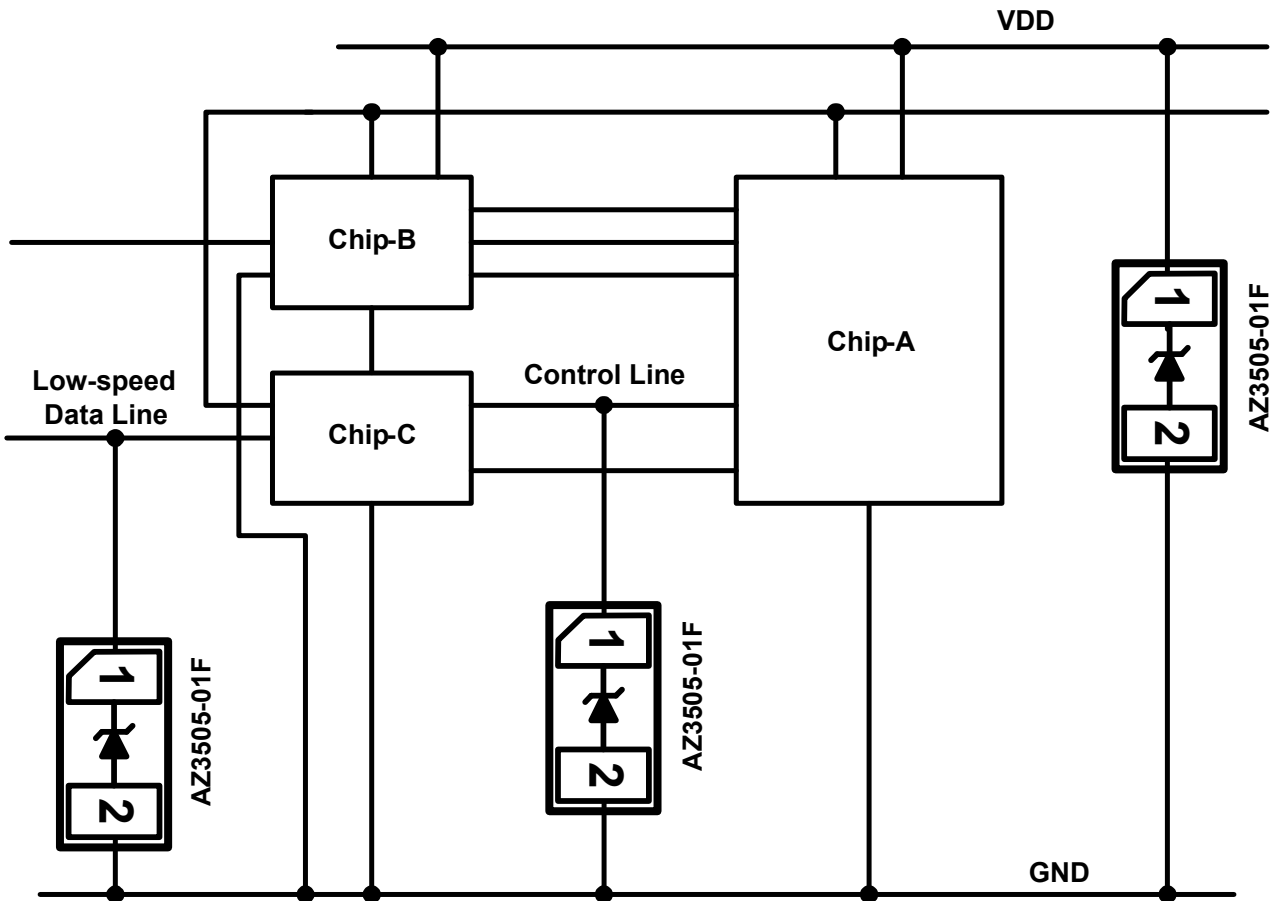
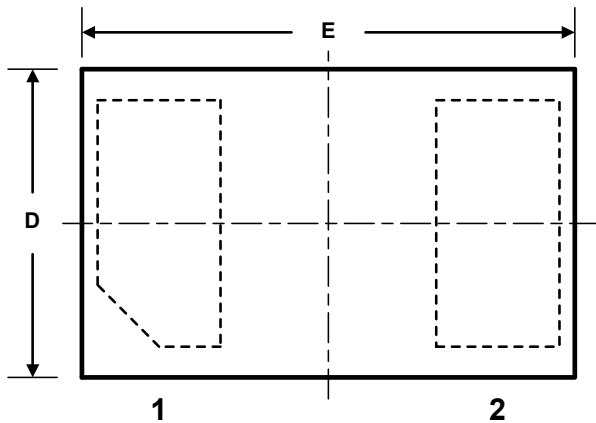


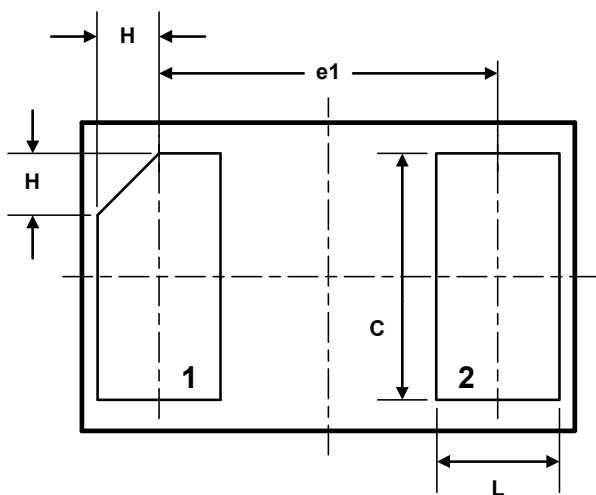
Fig. 2

Mechanical Details

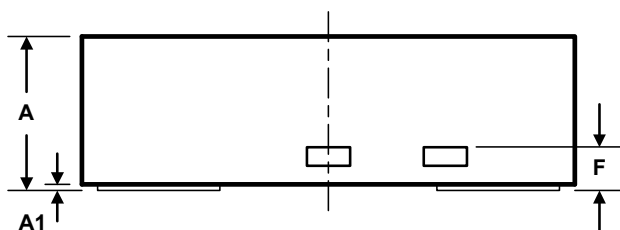
DFN1610P2E PACKAGE DIAGRAMS



Top View



Bottom View

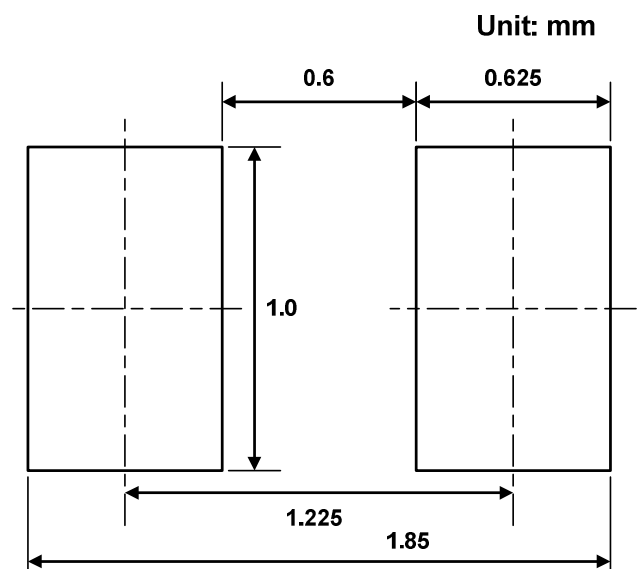


Side View

PACKAGE DIMENSIONS

SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
D	0.95	1.00	1.05
E	1.55	1.60	1.65
C	0.75	0.80	0.85
A	0.45	0.50	0.55
A1	-	0.02	0.05
e1	1.10BSC		
F	0.10	0.15	0.20
H	0.15	0.20	0.25
L	0.35	0.40	0.45

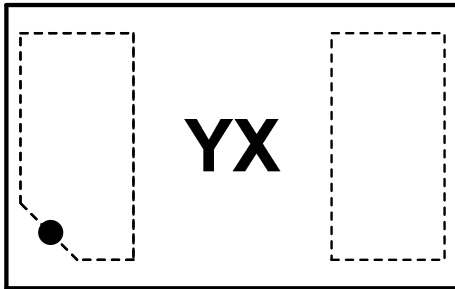
LAND LAYOUT



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



Top View

Y = Device Code
X = Date Code

Part Number	Marking Code
AZ3505-01F.R7G (Green Part)	YX

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ3505-01F.R7G	Green	T/R	7 inch	3,000/reel	4 reels = 12,000/box	6 boxes = 72,000/carton

Revision History

Revision	Modification Description
Revision 2017/12/27	Formal Release.