Features

- ESD protection for 4 high-speed I/O channels
- Protects 4 I/O lines operating up to **3.3V** and below
- Protects one VDD line operating up to **5V** and below
- Provide transient protection for each channel to
  IEC 61000-4-2 (ESD) ±30kV (air / contact)
  IEC 61000-4-4 (EFT) 80A (5/50ns)
  IEC 61000-4-5 (Lightning) 16A (8/20μs) for any I/O-to-GND
  IEC 61000-4-5 (Lightning) 22A (8/20μs) for VDD-to-GND
- Low capacitance: 1.7pF typical
- Fast turn-on and low clamping voltage
- Array of ESD rated diodes with internal equivalent TVS diode
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

- USB2.0 interface protection
- LVDS interface protection
- LAN applications
- General purpose I/O protection
- Notebook and PC computers

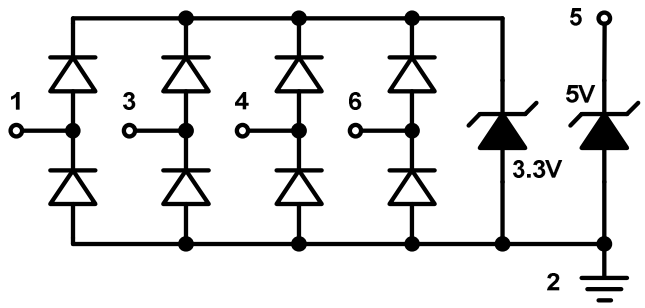
Description

AZ1235-04S is a high performance design which includes surge rated diode arrays to protect high speed data interfaces. The AZ1235-04S has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

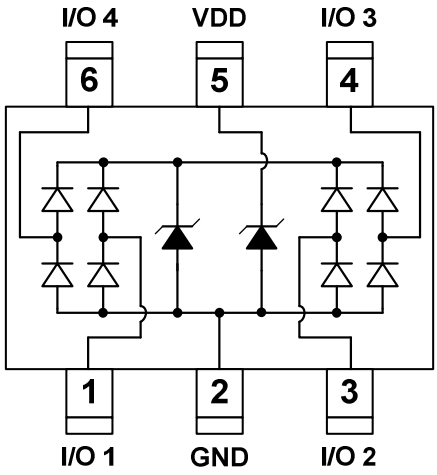
AZ1235-04S is a unique design which includes surge rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the internal ESD line or to the ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components.

AZ1235-04S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (± 15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



SOT23-6L (Top View)

Specifications

Absolute Maximum Ratings (T_A= 25°C, unless otherwise specified)			
Parameter	**Symbol**	**Rating**	**Unit**
Peak Pulse Current (t_p =8/20μs, I/O-to-GND) Peak Pulse Current (t_p =8/20μs, VDD-to-GND)	I_{PP-1} I_{PP-2}	16 22	A
Operating Voltage (I/O-to-GND) Operating Supply Voltage (VDD-to-GND)	V_{DC-1} V_{DC-2}	3.6 5.5	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD-1} V_{ESD-2}	±30 ±30	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +125	°C
Storage Temperature	T_{STO}	-55 to +150	°C

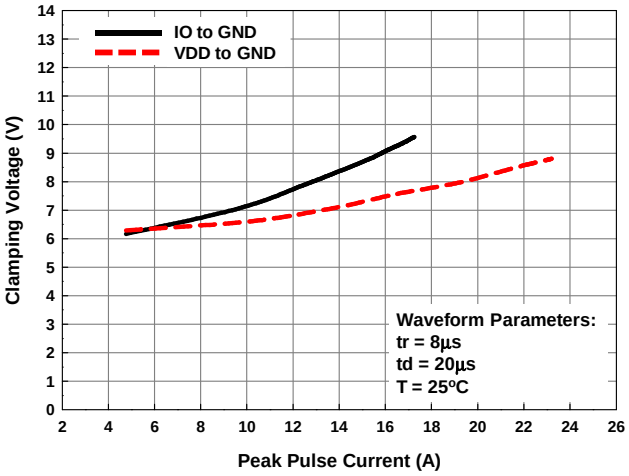
Electrical Characteristics						
Parameter	**Symbol**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Reverse Stand-Off Voltage	V_{RWM_VDD}	Pin-5 to pin-2, T = 25°C.			5	V
	$V_{RWM\_I/O}$	Pin-1, -3, -4, -6 to pin-2, T = 25°C.			3.3	V
Reverse Leakage Current	I_{Leak_VDD}	V_{Pin-5} = 5V, V_{Pin-2} = 0V, T = 25°C.			1	μA
Channel Leakage Current	$I_{Leak\_I/O}$	$V_{Pin-1,-3,-4,-6}$ = 3.3V, V_{Pin-2} = 0V, T = 25°C.			0.5	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T = 25°C, pin-5 to pin-2.	6		9	V
Forward Voltage	V_F	I_F = 15mA, T = 25°C, pin-2 to pin-5.	0.6		1.2	V
ESD Clamping Voltage - I/O (Note 1)	$V_{CL-ESD\_I/O}$	IEC 61000-4-2 +8kV (I_{TLP} = 16A), contact mode, T = 25 °C, any I/O pin to GND.		7.5		V
ESD Clamping Voltage - VDD (Note 1)	V_{CL-ESD_VDD}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), contact mode, T = 25 °C, VDD pin to GND.		6.5		V
ESD Dynamic Turn-on Resistance - I/O	$R_{dynamic\_I/O}$	IEC 61000-4-2, 0~+8kV, T = 25°C, contact mode, any I/O pin to GND.		0.14		Ω
ESD Dynamic Turn-on Resistance - VDD	$R_{dynamic\_VDD}$	IEC 61000-4-2, 0~+8kV, T = 25°C, contact mode, VDD pin to GND.		0.05		Ω

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.
TLP conditions: Z_0 = 50Ω, t_p = 100ns, t_r = 1ns.

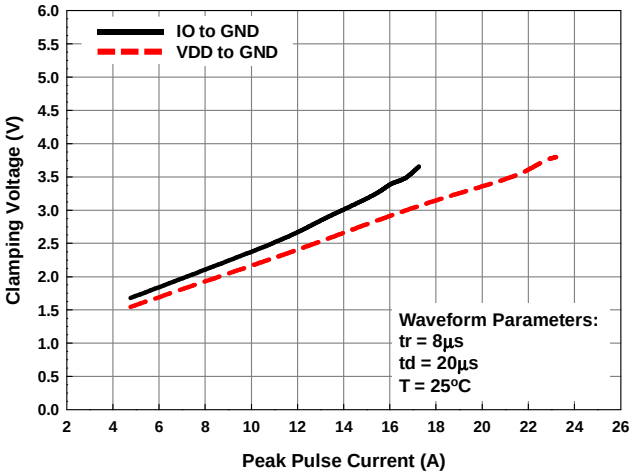
Electrical Characteristics						
Parameter	**Symbol**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Surge Clamping Voltage - I/O	$V_{CL-surge-I/O}$	I_{PP} = 5A, t_p = 8/20μs, T = 25 °C, any I/O pin to GND.		6		V
		I_{PP} = 16A, t_p = 8/20μs, T = 25 °C, any I/O pin to GND.		9.2		V
Surge Clamping Voltage - VDD	$V_{CL-surge-VDD}$	I_{PP} = 5A, t_p = 8/20μs, T = 25 °C, VDD pin to GND.		6		V
		I_{PP} = 22A, t_p = 8/20μs, T = 25 °C, VDD pin to GND.		8.5		V
Channel Input Capacitance	C_{IN}	V_{IN} = 1.65V, V_{Pin-2} = 0V, T = 25°C, f = 1MHz, any I/O pin to GND.		1.7	2	pF
Channel to Channel Input Capacitance	$C_{I/O-to-I/O}$	V_{IN} = 1.65V, V_{Pin-2} = 0V, T = 25°C, f = 1MHz, between I/O pins.		0.15	0.25	pF

Typical Characteristics

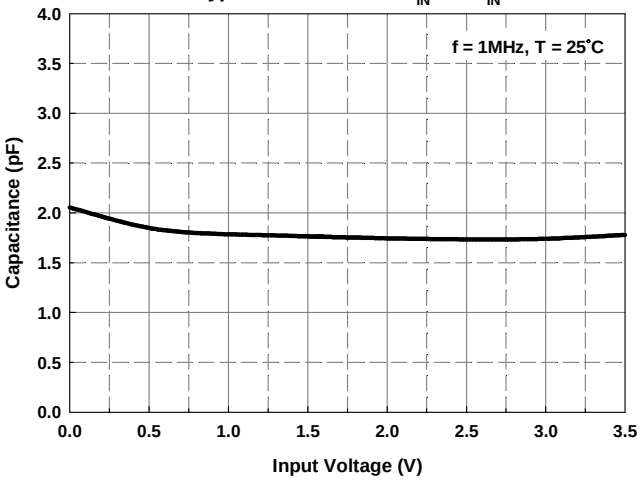
Reverse Clamping Voltage vs. Peak Pulse Current



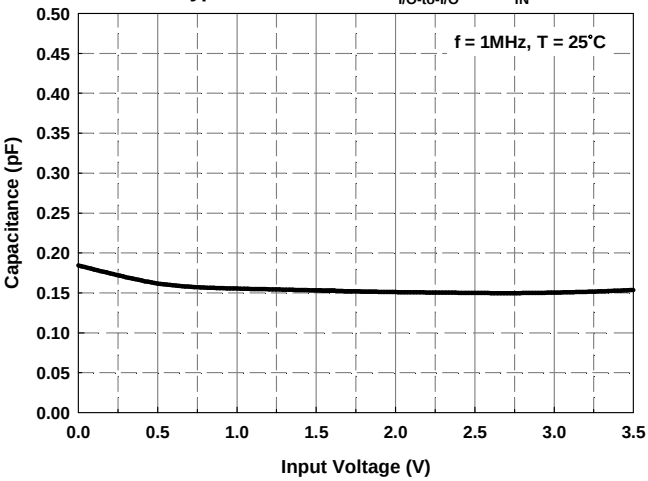
Forward Clamping Voltage vs. Peak Pulse Current



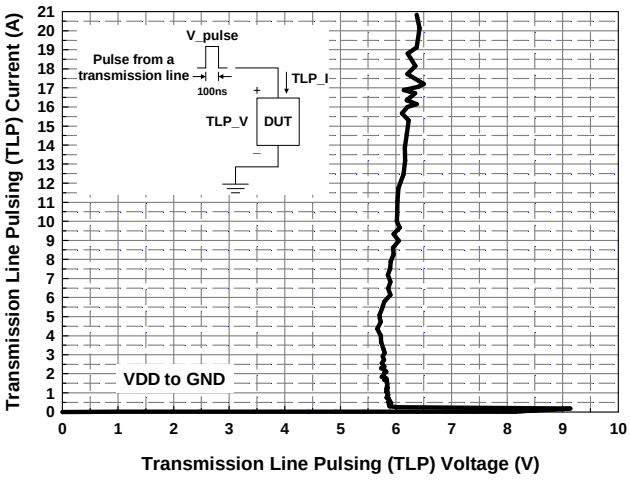
Typical Variation of C_{IN} vs. V_{IN}



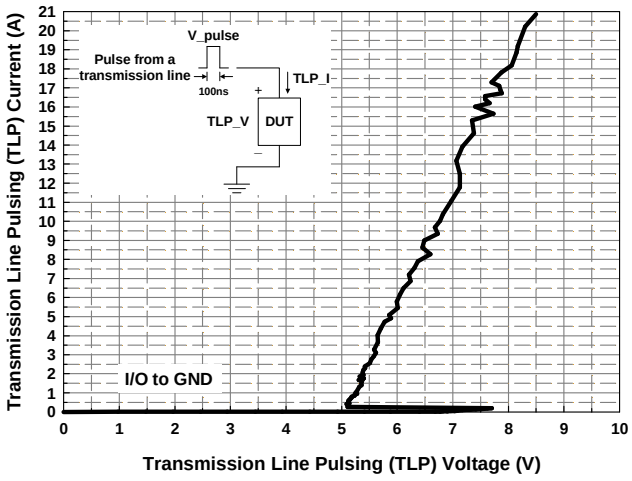
Typical Variation of $C_{I/O\text{-}to\text{-}I/O}$ vs. V_{IN}



Transmission Line Pulsing (TLP) Measurement



Transmission Line Pulsing (TLP) Measurement



Applications Information

Device Connection

The AZ1235-04S is designed to protect four data lines and one power rail from transient over-voltage (such as ESD stress pulse). The device connection of AZ1235-04S is shown in the Fig. 1. In Fig. 1, the four protected data lines are connected to the ESD protection pins (pin-1, pin-3, pin-4, and pin-6) of AZ1235-04S. The ground pin (pin-2) of AZ1235-04S is a negative reference pin. This pin should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible. In addition, the power pin (pin-5) of AZ1235-04S is a positive reference pin. This pin should directly connect to the VDD rail of PCB., then the VDD rail also can be protected by the power-rail ESD clamped circuit (not shown) of AZ1235-04S.

AZ1235-04S can provide protection for 4 I/O signal lines simultaneously. If the number of I/O signal lines is less than 4, the unused I/O pins can be simply left as NC pins.

In some cases, systems are not allowed to be reset or restart after the ESD stress directly applying at the I/O-port connector. Under this situation, in order to enhance the sustainable ESD Level, a 0.1μF chip capacitor can be added between the VDD and GND rails. The place of this chip capacitor should be as close as possible to the AZ1235-04S.

In some cases, there isn't power rail presented on the PCB. Under this situation, the power pin (pin-5) of AZ1235-04S can be left as floating. The protection will not be affected. Fig. 2 shows the detail connection.

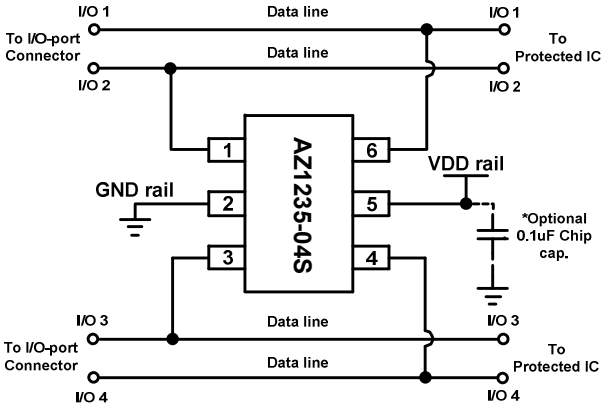


Fig. 1 Data lines and power rails connection of AZ1235-04S.

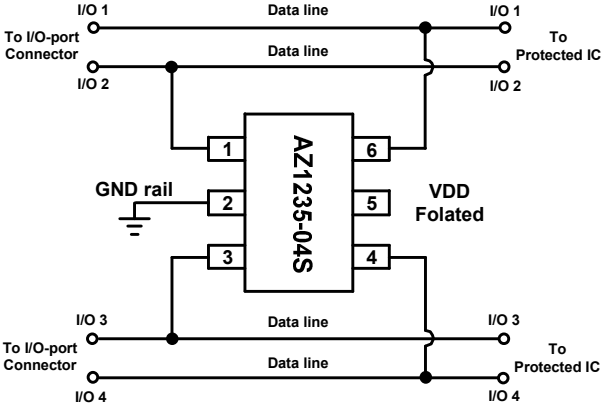
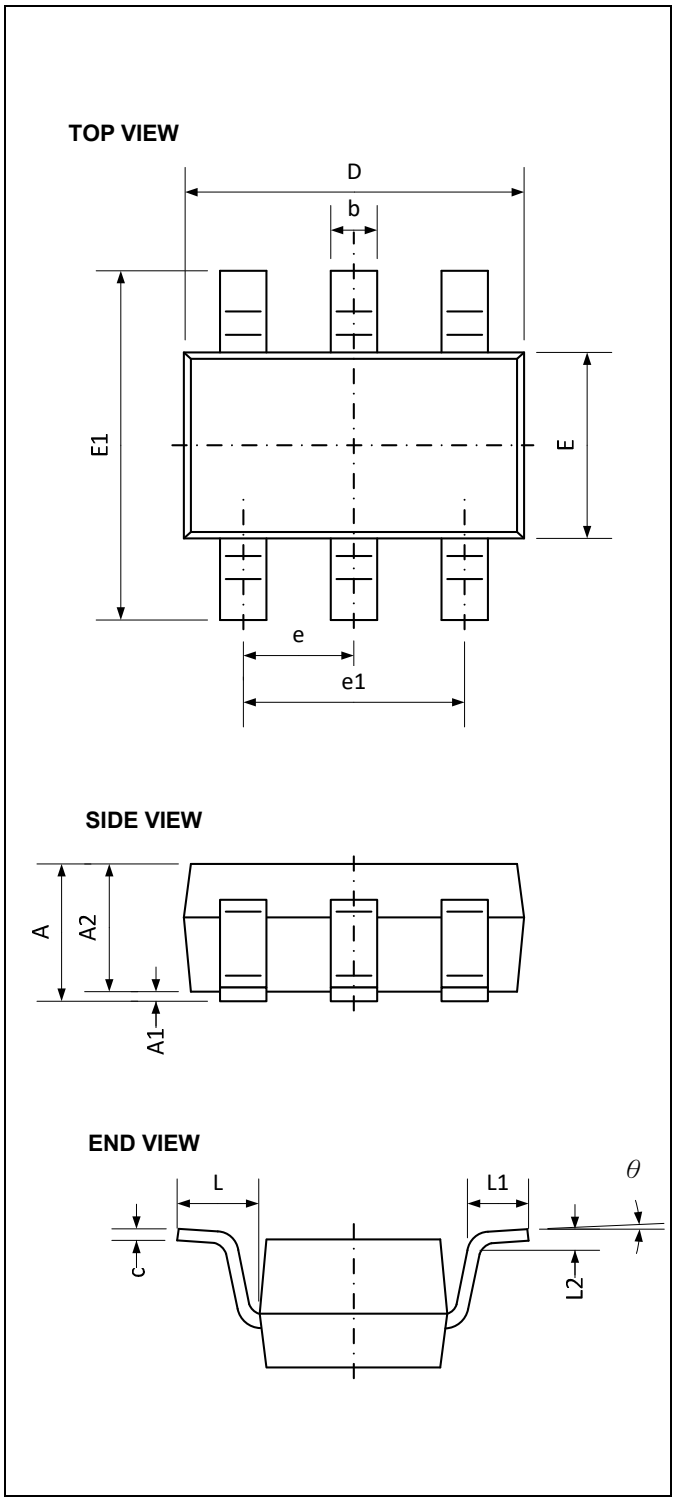


Fig. 2 Data lines and power rails connection of AZ1235-04S. VDD pin is left as floating when no power rail presented on the PCB.

Mechanical Details

SOT23-6L

Package Diagrams



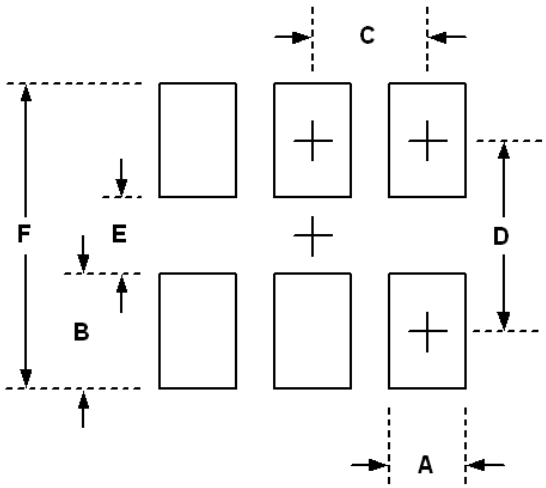
Package Dimensions

Symbol	Millimeters	
	Min.	Max.
A	-	1.25
A1	0.00	0.10
A2	0.90	1.20
b	0.30	0.50
c	0.08	0.21
D	2.72	3.12
E	1.40	1.80
E1	2.60	3.00
e	0.95 BSC	
e1	1.90 BSC	
L1	0.30	0.60
L	0.70 REF	
L2	0.25 BSC	
θ	0	8

Notes:

- This dimension complies with JEDEC outline standard MO-178 Variation AB.
- Dimensioning and tolerancing per ASME Y14.5M-1994.
- All dimensions are in millimeters.

Land Layout

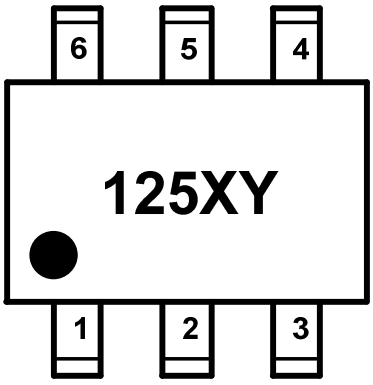


Dimensions		
Index	**Millimeter**	**Inches**
A	0.60	0.024
B	1.10	0.043
C	0.95	0.037
D	2.50	0.098
E	1.40	0.055
F	3.60	0.141

Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

Marking Code



125 = Device Code

X = Date Code

Y = Control Code

Part Number	Marking Code
AZ1235-04S.R7G (Green part)	125XY

Note : Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ1235-04S.R7G	Green	T/R	7 inch	3,000/reel	4 reels = 12,000/box	6 boxes = 72,000/carton

Revision History

Revision	Modification Description
Revision 2019/11/07	Formal Release.