Features

- ESD Protect for Super Speed Differential Signaling (above 5Gb/s) channels
- **Protects six I/O lines operating up to 3.3V and below**
- **Protects one V_{DD} line operating up to 5.0V and below**
- Provide ESD protection for each channel to **IEC 61000-4-2 (ESD) ±15kV (air), ±10kV (contact)**
- **Ultra low capacitance: 0.45pF typ.**
- Fast turn-on and Low clamping voltage
- Array of surge rated diodes with internal equivalent TVS diode
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

- **USB3.0**
- **High Speed I/O Ports in Any Electronic Product**

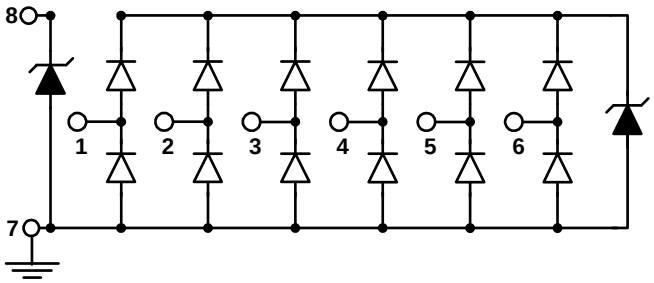
Description

AZ1165-06Q is a design which includes ESD rated diode arrays to protect high speed data interfaces. The AZ1165-06Q has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD).

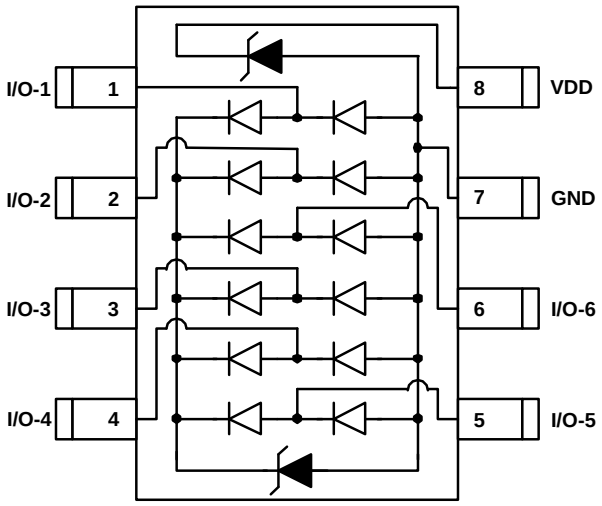
AZ1165-06Q is a unique design which includes surge rated, ultra low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the power supply line or to ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components.

AZ1165-06Q may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



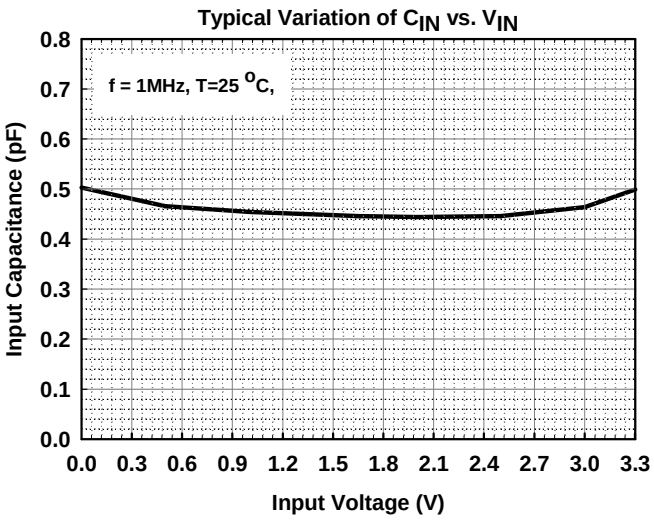
MSOP-8L (Top View)

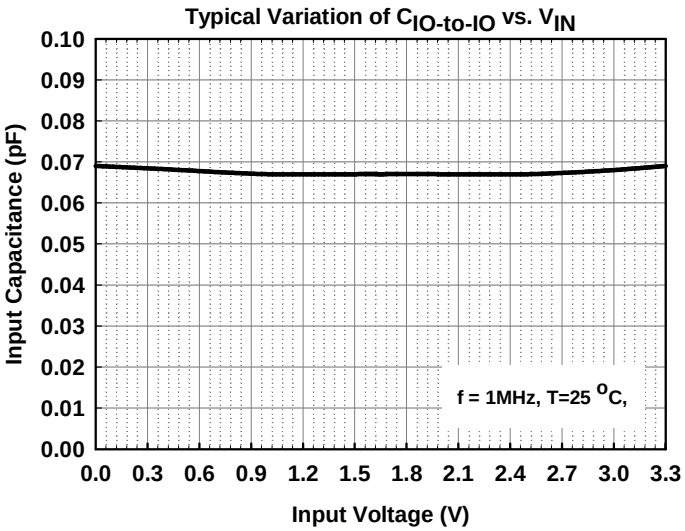
SPECIFICATIONS

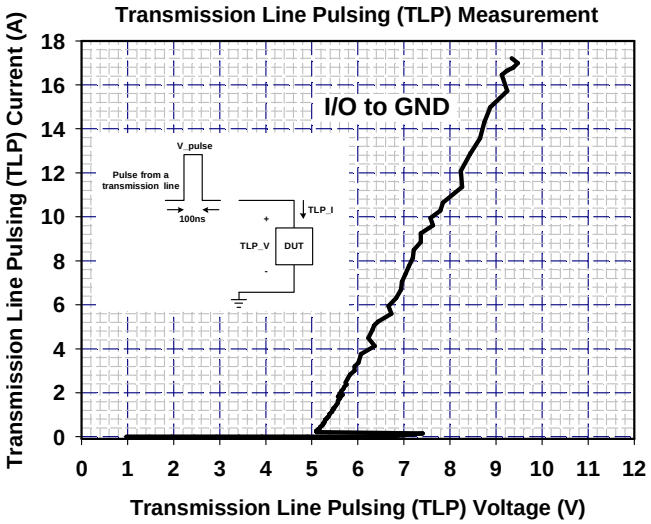
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNITS**
Operating Voltage (I/O-GND) Operating Supply Voltage (VDD-GND)	**V_{DC}**	3.6 5.5	**V**
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	**V_{ESD}**	±15 ±10	**kV**
Lead Soldering Temperature	**T_{SOL}**	260 (10 sec.)	**°C**
Operating Temperature	**T_{OP}**	-40 to +85	**°C**
Storage Temperature	**T_{STO}**	-55 to +150	**°C**
DC Voltage at any I/O pin	**V_{IO}**	(GND – 0.5) to (VDD + 0.5)	**V**

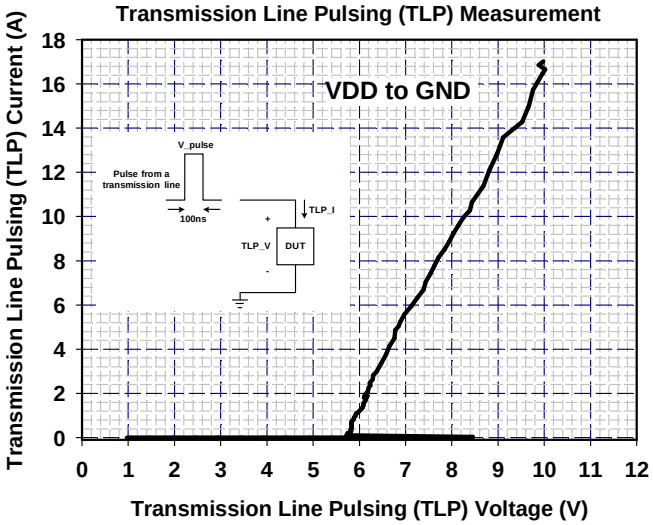
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM_VDD}	Pin-8 to pin-7, T=25 °C			5	**V**
	V_{RWM_IO}	Pin-1~6 to pin-7, T=25 °C			3.3	
Reverse Leakage Current	I_{Leak_VDD}	V_{Pin-8} = 5V, V_{Pin-7} = 0V, T=25 °C			2.5	**µA**
Channel Leakage Current	I_{Leak_IO}	$V_{Pin-1~6}$ = 3.3V, V_{Pin-7} = 0V, T=25 °C			1	**µA**
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, pin-8 to pin-7	6		9.5	**V**
Forward Voltage	V_F	I_F = 15mA, T=25 °C, pin-7 to pin-8		0.8	1.2	**V**
ESD Clamping Voltage –I/O	V_{Cclamp_IO}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, any I/O pin to Ground		9.5		**V**
ESD Clamping Voltage –VDD	V_{clamp_VDD}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, VDD pin to Ground		10		**V**
ESD Dynamic Turn-on Resistance –I/O	$R_{dynamic\_IO}$	IEC 61000-4-2, 0~+6kV,T=25 °C, Contact mode, any I/O pin to Ground		0.25		**Ω**
ESD Dynamic Turn-on Resistance –VDD	$R_{dynamic\_VDD}$	IEC 61000-4-2, 0~+6kV, T=25 °C, Contact mode, VDD pin to Ground		0.25		**Ω**
Channel Input Capacitance	C_{IN}	V_{pin-7} = 0V, **V_{IN} = 1.65V**,f = 1MHz, T=25 °C, any I/O pin to Ground		0.45	0.6	**pF**
Channel to Channel Input Capacitance	C_{CROSS}	V_{pin-7} = 0V, **V_{IN} = 1.65V**, f = 1MHz, T=25 °C, between I/O pins		0.07	0.10	**pF**

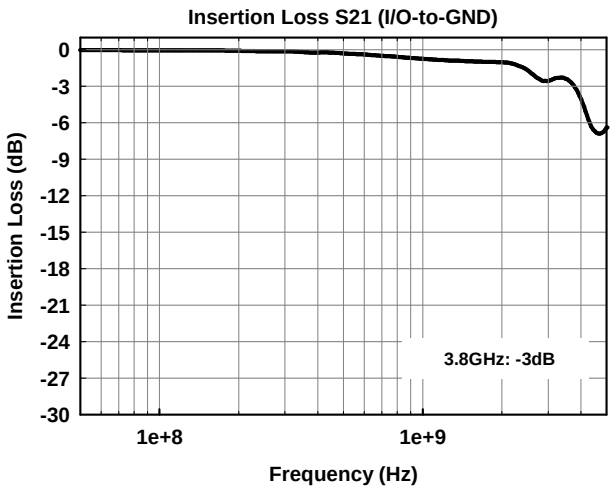
Typical Characteristics

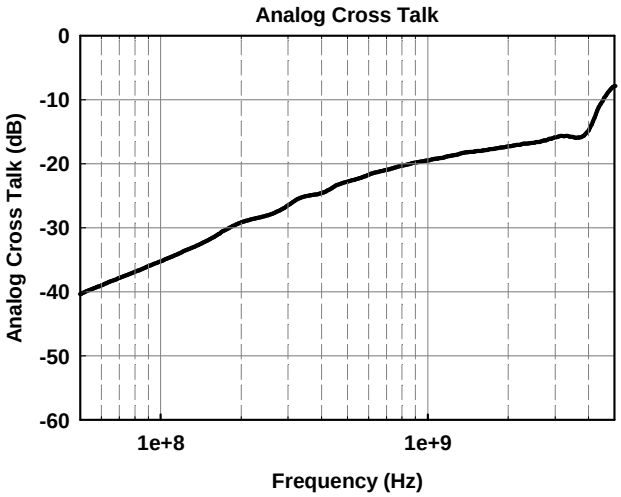












Applications Information

A. Device Connection

The AZ1165-06Q is designed to protect six data lines and one power rail from transient over-voltage (such as ESD stress pulse). The device connection of AZ1165-06Q is shown in the Fig. 1. In Fig. 1, the six protected data lines are connected to the ESD protection pins (pin1, pin2, pin3, pin4, pin5, and pin6) of AZ1165-06Q. The ground pin (pin7) of AZ1165-06Q is a negative reference pin. This pin should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible. In addition, the power pin (pin 8) of AZ1165-06Q is a positive reference pin. This pin should directly connect to the VDD rail of PCB., then the VDD rail also can be protected by the power-rail ESD clamped circuit (not shown) of AZ1165-06Q.

AZ1165-06Q can provide protection for 6 I/O signal lines simultaneously. If the number of I/O signal lines is less than 6, the unused I/O pins can be simply left as NC pins.

In some cases, systems are not allowed to be reset or restart after the ESD stress directly applying at the I/O-port connector. Under this situation, in order to enhance the sustainable ESD Level, a 0.1μF chip capacitor can be added between the VDD and GND rails. The place of this chip capacitor should be as close as possible to the AZ1165-06Q.

In some cases, there isn't power rail presented on the PCB. Under this situation, the power pin (pin 8) of AZ1165-06Q can be left as floating. The protection will not be affected, only the load capacitance of I/O pins will be slightly increased. Fig. 2 shows the detail connection.

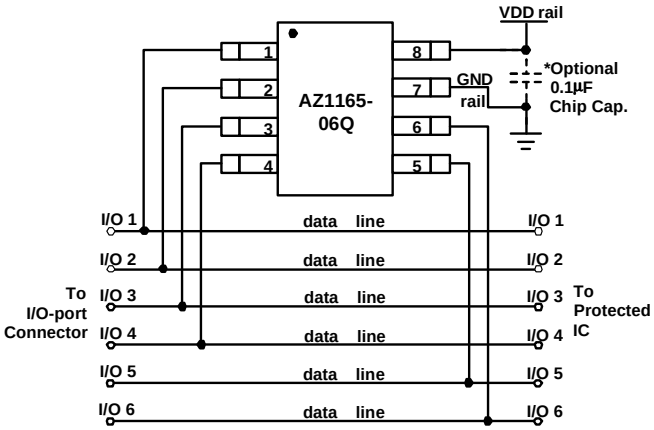


Fig. 1 Data lines and power rails connection of AZ1165-06Q.

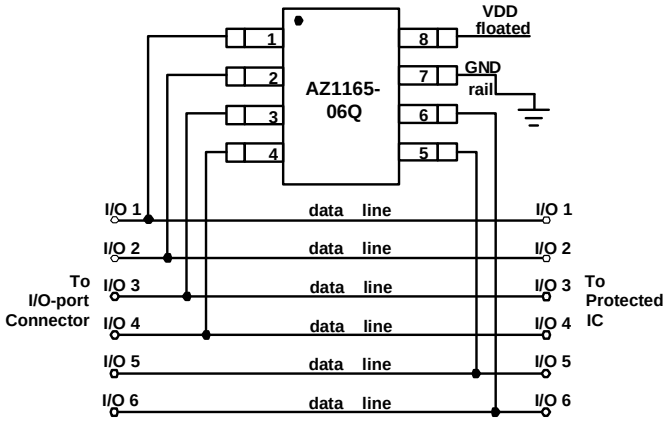
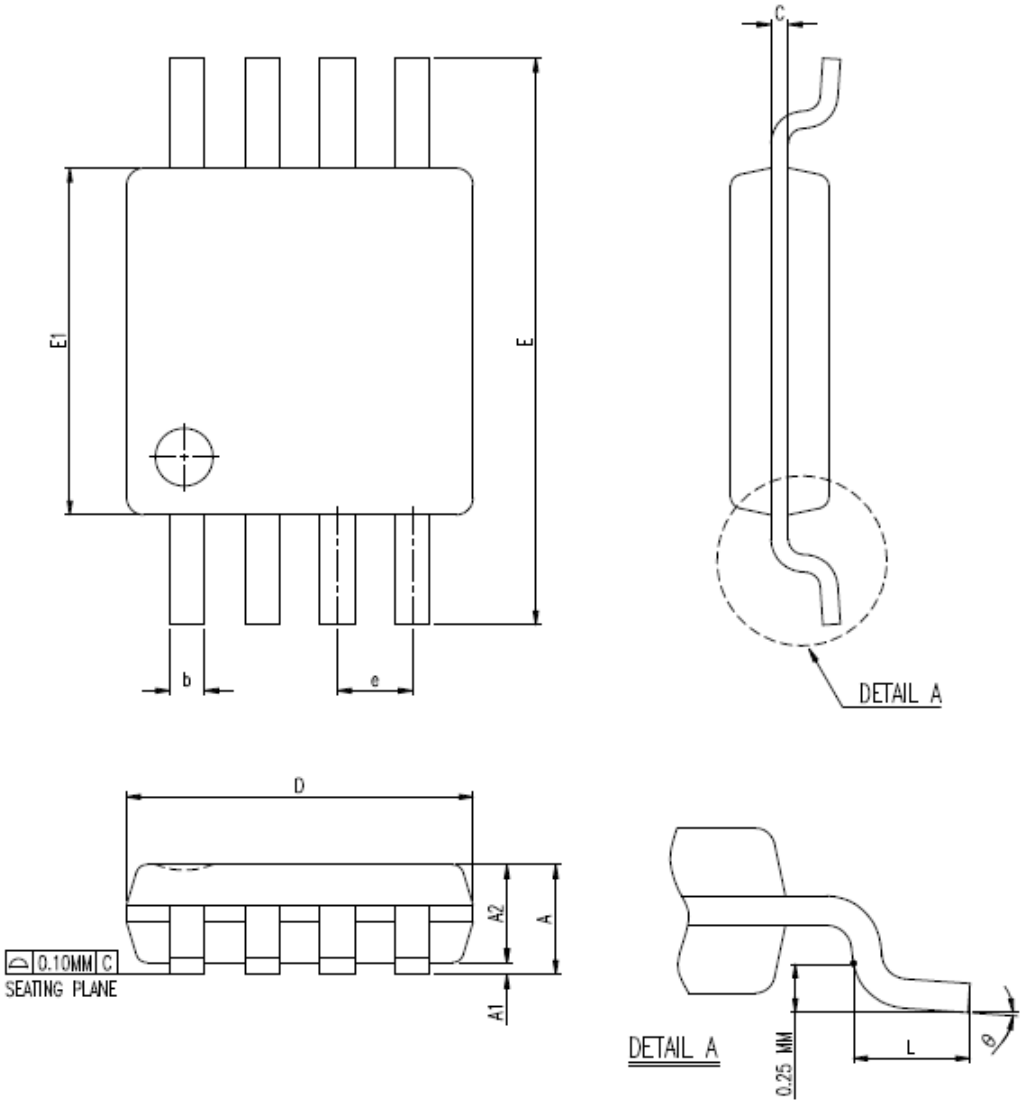


Fig. 2 Data lines and power rails connection of AZ1165-06Q. VDD pin is left as floating when no power rail presented on the PCB.

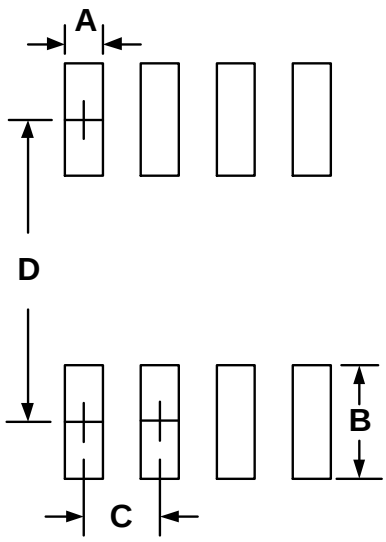
PACKAGE OUTLINE



Symbol	Millimeters		Inches	
	min	max	min	max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.750	0.970	0.030	0.038
b	0.280	0.380	0.011	0.015
C	0.130	0.230	0.005	0.009
D	2.900	3.100	0.114	0.122
e	0.65 BASIC		0.026 BASIC	
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
L	0.400	0.700	0.016	0.028
θ	0°	8°	0°	8°

*NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS.
MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 INCH (0.15 MM) PER SIDE .
DIMENSION " E1 " DOES NOT INCLUDE MOLD PROTRUSIONS
MOLD PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.25 MM) PER SIDE .

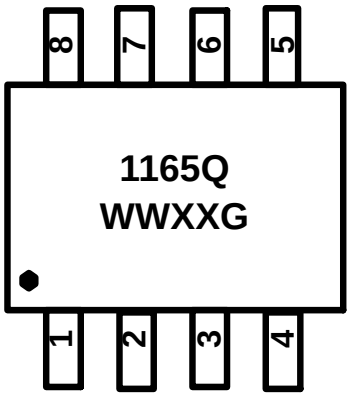
LAND LAYOUT



Dimensions		
Index	**Millimeter**	**Inches**
A	0.41	0.016
B	1.02	0.040
C	0.65	0.023
D	4.8	0.189

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



1165Q = Device Code
WW = Date Code
XX = Control Code
G = Green part

Part Number	Marking Code
AZ1165-06Q	**1165Q**

Revision History

Revision	Modification Description
Revision 2013/06/11	Formal Release.