Features

- ESD protect for 8 high-speed I/O channels
- Provide transient protection for each channel to
  IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-5 (Lightning) 3A (8/20μs)
- **For low operating voltage of 1.5V and below**
- **Ultra-low capacitance: 0.1pF typical**
- Fast turn-on and low clamping voltage
- Array of ESD rated diodes with internal equivalent TVS (Transient Voltage Suppression) diode
- Solid-state silicon-avalanche and active circuit triggering technology
- Simplified layout for high-speed differential signaling channels
- ***Green part***

Applications

- V-by-One interface
- LVDS Interface
- USB 3.0 and USB 3.1 interfaces
- DisplayPort interface
- SATA and eSATA interfaces

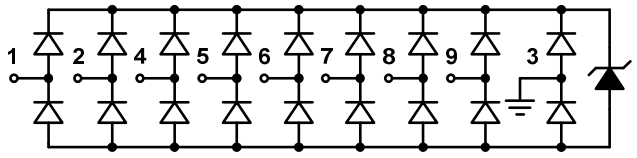
Description

AZ111S-08F is a design which includes ESD rated diode arrays to protect high speed data interfaces. The AZ111S-08F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD).

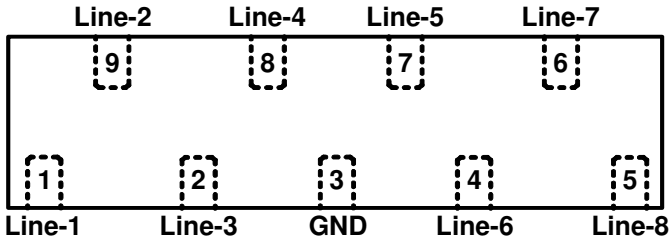
AZ111S-08F is a unique design which includes ESD rated, ultra-low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to the ground line. The internal unique design of clamping cell prevents over-voltage on the I/O line, protecting any downstream components.

AZ111S-08F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



DFN3810P9E
(Top View)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A= 25°C, unless otherwise specified)			
PARAMETER	**SYMBOL**	**RATING**	**UNIT**
Peak Pulse Current (tp = 8/20μs)	I_{PP}	3	A
Operating Voltage (I/O pin-GND)	V_{DC}	±1.65	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD-1} V_{ESD-2}	±15 ±8	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +125	°C
Storage Temperature	T_{STO}	-55 to +150	°C

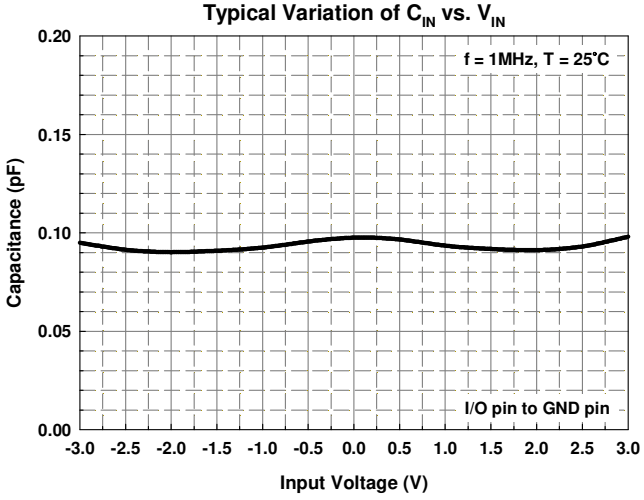
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITION**	**MIN**	**TYP**	**MAX**	**UNIT**
Reverse Stand-Off Voltage	V_{RWM}	Any I/O pin to GND, T=25 °C.			1.5	V
Reverse Leakage Current	$I_{CH-Leak}$	V_{RWM} = 1.5V, T=25 °C, any I/O pin to GND.			0.5	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, any I/O pin to GND.	4.5			V
ESD Clamping Voltage (Note 1)	V_{CL-ESD}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), contact mode, any I/O pin to GND, T=25 °C.		15		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2, 0~+8kV, contact mode, any I/O pin to GND, T=25 °C.		0.7		Ω
Channel Input Capacitance	C_{IN}	V_{pin-3} = 0V, V_{IN} = 0V, f =1MHz, T=25 °C, any I/O pin to GND.		0.10	0.15	pF
Channel to Channel Input Capacitance	C_{CROSS}	V_{pin-3} = 0V, V_{IN} = 0V, f = 1MHz, T=25 °C, between I/O pins.		0.10	0.15	pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

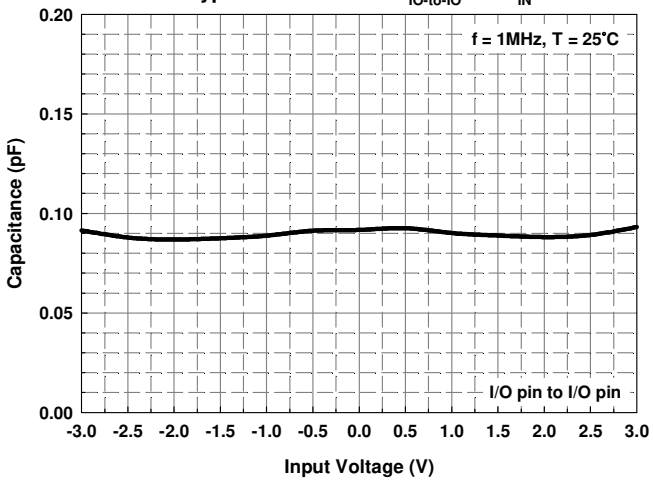
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics

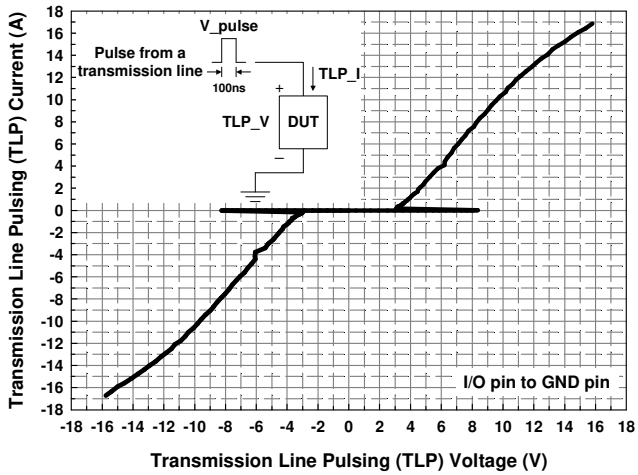
Typical Variation of C_{IN} vs. V_{IN}



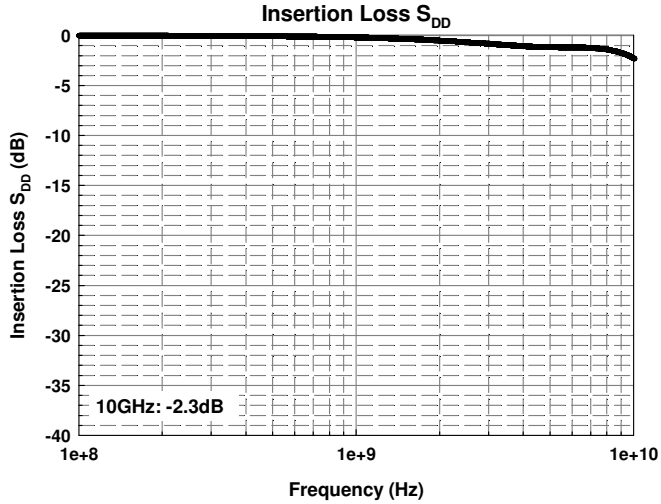
Typical Variation of $C_{IO\text{-}to\text{-}IO}$ vs. V_{IN}



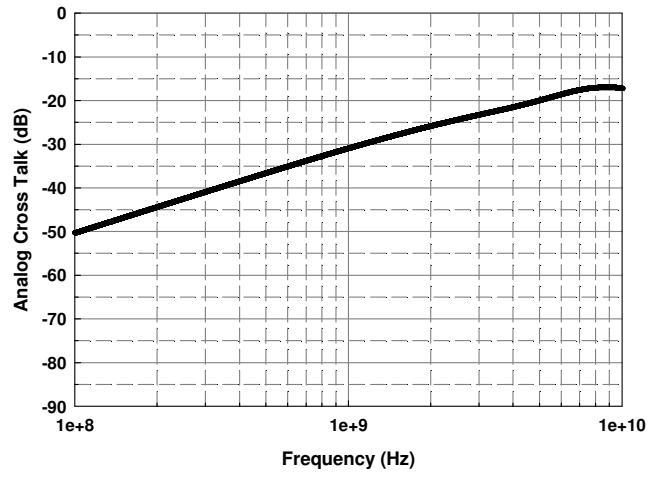
Transmission Line Pulsing (TLP) Measurement



Insertion Loss S_{DD}



Analog Cross Talk



Application Information

The AZ111S-08F is designed to protect 8 high-speed data lines from transient over-voltage (such as ESD stress pulse). The device connection of AZ111S-08F is shown in the Fig. 1. In Fig. 1, the 8 protected high-speed data lines are connected to the ESD protection pins (pin1, pin2, pin4, pin5, pin6, pin7, pin8, and pin9) of AZ111S-08F. The AZ111S-08F is designed for allowing the traces to run straight through the device to simplify the PCB layout. The ground pin (pin3) of AZ111S-08F is a negative reference pin. This pin should be directly connected to the GND rail of PCB. To get minimum parasitic inductance, the path length should keep as short as possible.

AZ111S-08F can provide ESD protection for 8 I/O signal lines simultaneously. If the number of I/O signal lines is less than 8, the unused I/O pins can be simply left as NC pins.

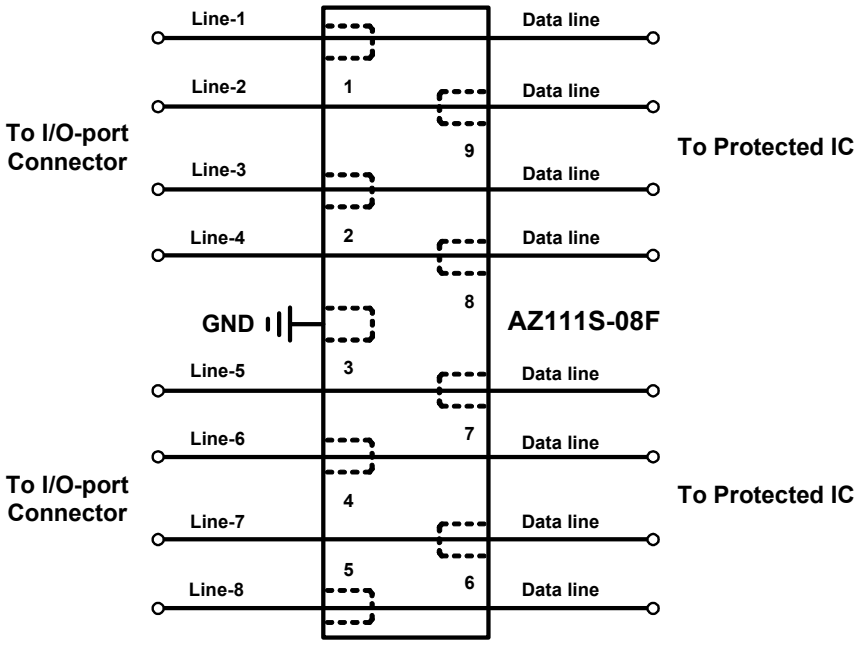


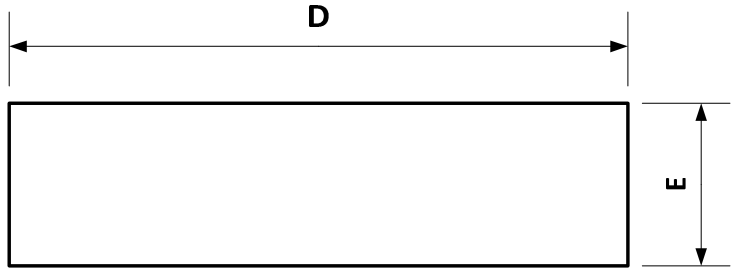
Fig. 1 Data lines connection of AZ111S-08F.

Mechanical Details

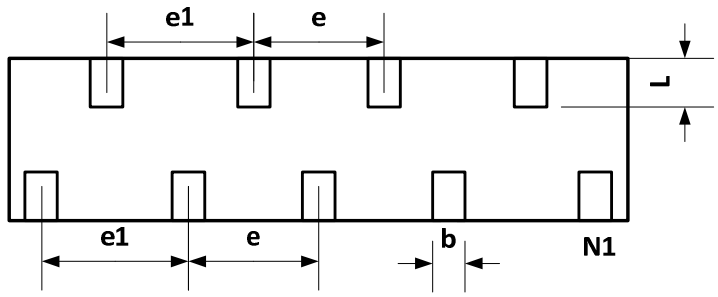
DFN3810P9E

PACKAGE DIAGRAMS AND DIMENSIONS

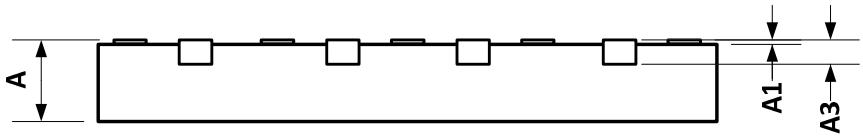
TOP VIEW



BOTTOM VIEW

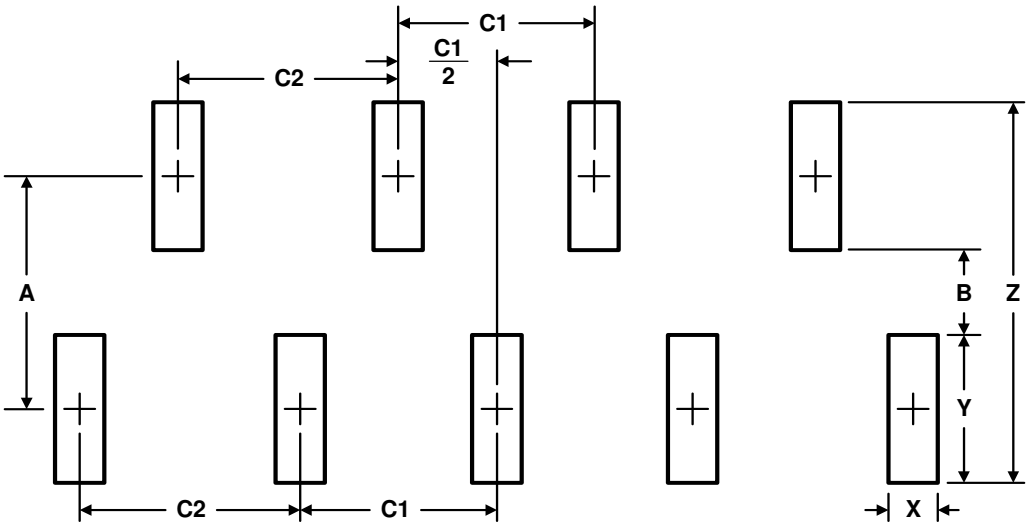


SIDE VIEW



SYMBOL	MILLIMETERS	
	MIN.	MAX.
A	0.45	0.55
A1	0.00	0.05
A3	0.15 REF.	
D	3.70	3.90
E	0.90	1.10
b	0.15	0.25
e	0.80 TYP.	
e1	0.90 TYP.	
L	0.20	0.40

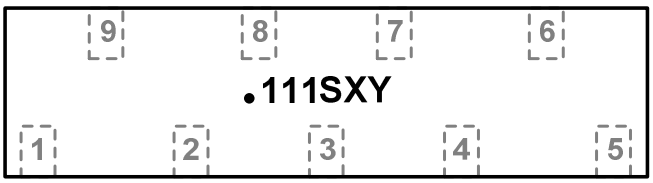
LAND LAYOUT



Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

Dimensions	
Index	**Millimeters**
A	0.95
B	0.35
C1	0.80
C2	0.90
X	0.20
Y	0.60
Z	1.55

MARKING CODE



111S=Device Code
X=Date Code
Y=Control Code

Part Number	Marking Code
AZ111S-08F.R7G (Green Part)	111SXY

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Real Size	MOQ	MOQ / internal box	MOQ / carton
AZ111S-08F.R7G	Green	T/R	7 inch	3,000/reel	3 reels = 9,000/box	6 boxes = 54,000/carton

Revision History

Revision	Modification Description
Revision 2019/01/14	Formal release.