



## Features

- ESD protection for one line with bi-direction
- Provide transient protection for one line to **IEC 61000-4-2 (ESD)  $\pm 30\text{kV}$  (air),  $\pm 24\text{kV}$  (contact)**  
**IEC 61000-4-5 (Lightning) 7A (8/20 $\mu\text{s}$ )**
- Suitable for, **12V** and below, operating voltage applications
- Low capacitance: 2.0pF typical
- Fast turn-on and low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green part**
- **AEC-Q101 qualified**

## Applications

- Automotive application
- Power management system
- Industrial system
- Portable instrumentation
- Peripherals

## Description

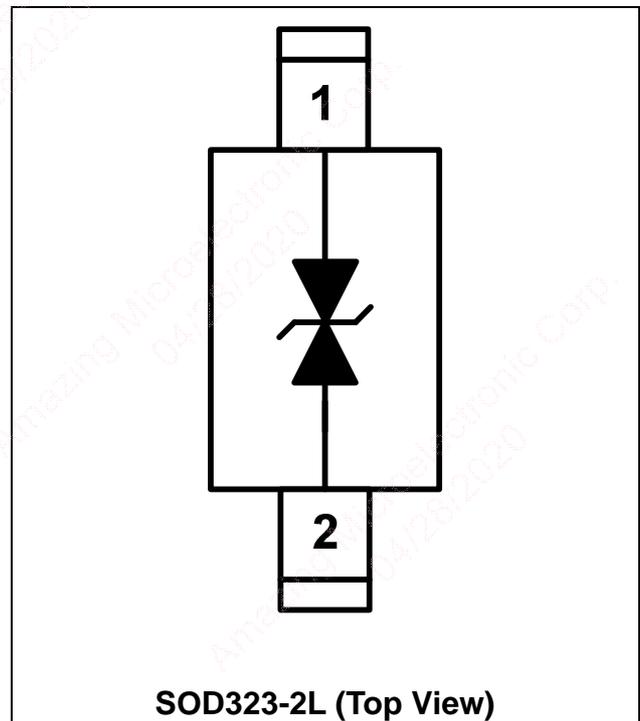
AZ9812-01L is a design which includes a bi-directional ESD rated clamping cell to protect one power line, or one control line, or one high-speed data line in an electronic system. The AZ9812-01L has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage caused by Electrostatic

Discharging (ESD), Lightning, and Cable Discharge Event (CDE).

AZ9812-01L is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line, control line or data line, protecting any downstream components.

AZ9812-01L may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ( $\pm 15\text{kV}$  air,  $\pm 8\text{kV}$  contact discharge).

## Circuit Diagram / Pin Configuration





## Specifications

Absolute Maximum Ratings			
Parameter	Symbol	Rating	Unit
Peak Pulse Current ( $t_p=8/20\mu s$ )	$I_{PP}$	7	A
Operating Voltage	$V_{DC}$	$\pm 13.2$	V
ESD per IEC 61000-4-2 (Air)	$V_{ESD-1}$	$\pm 30$	kV
ESD per IEC 61000-4-2 (Contact)	$V_{ESD-2}$	$\pm 24$	
Lead Soldering Temperature	$T_{SOL}$	260 (10 sec.)	$^{\circ}C$
Operating Temperature	$T_{OP}$	-55 to +125	$^{\circ}C$
Storage Temperature	$T_{STO}$	-55 to +150	$^{\circ}C$

Electrical Characteristics						
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	$V_{RWM}$	$T = 25^{\circ}C$ .	-12		12	V
Reverse Leakage Current	$I_{Leak}$	$V_{RWM} = \pm 12V, T = 25^{\circ}C$ .			1	$\mu A$
Reverse Breakdown Voltage	$V_{BV}$	$I_{BV} = 1mA, T = 25^{\circ}C$ .	13.5		16.5	V
Surge Clamping Voltage	$V_{CL-surge}$	$I_{PP} = 7A, t_p = 8/20\mu s, T = 25^{\circ}C$ .		19		V
ESD Clamping Voltage (Note 1)	$V_{CL-ESD}$	IEC 61000-4-2, +8kV ( $I_{TLP} = 16A$ ), contact mode, $T = 25^{\circ}C$ .		22		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2, 0~+8kV, contact mode, $T = 25^{\circ}C$ .		0.4		$\Omega$
Channel Input Capacitance	$C_{IN}$	$V_R = 0V, f = 1MHz, T = 25^{\circ}C$ .		2	2.5	pF

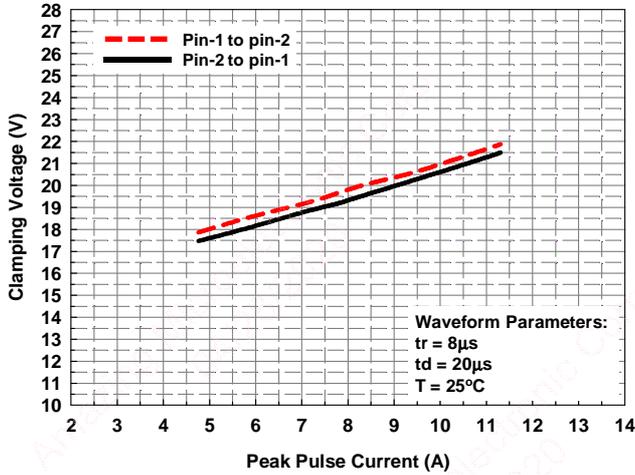
Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions:  $Z_0 = 50\Omega, t_p = 100ns, t_r = 1ns$ .

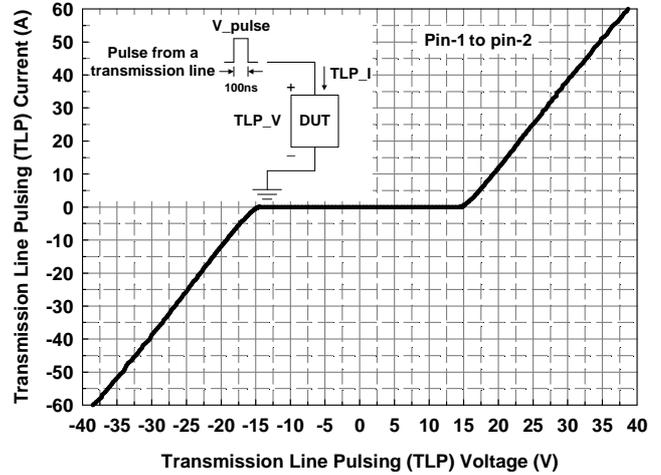


## Typical Characteristics

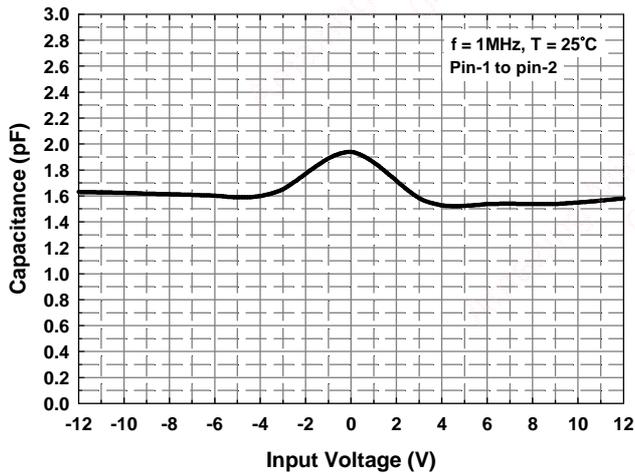
Reverse Clamping Voltage vs. Peak Pulse Current



Transmission Line Pulsing (TLP) Measurement



Typical Variation of  $C_{IN}$  vs.  $V_{IN}$





## Application Information

The AZ9812-01L is designed to protect one line against system ESD/Lightning pulses by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ9812-01L is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ9812-01L should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ9812-01L.
- Place the AZ9812-01L near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

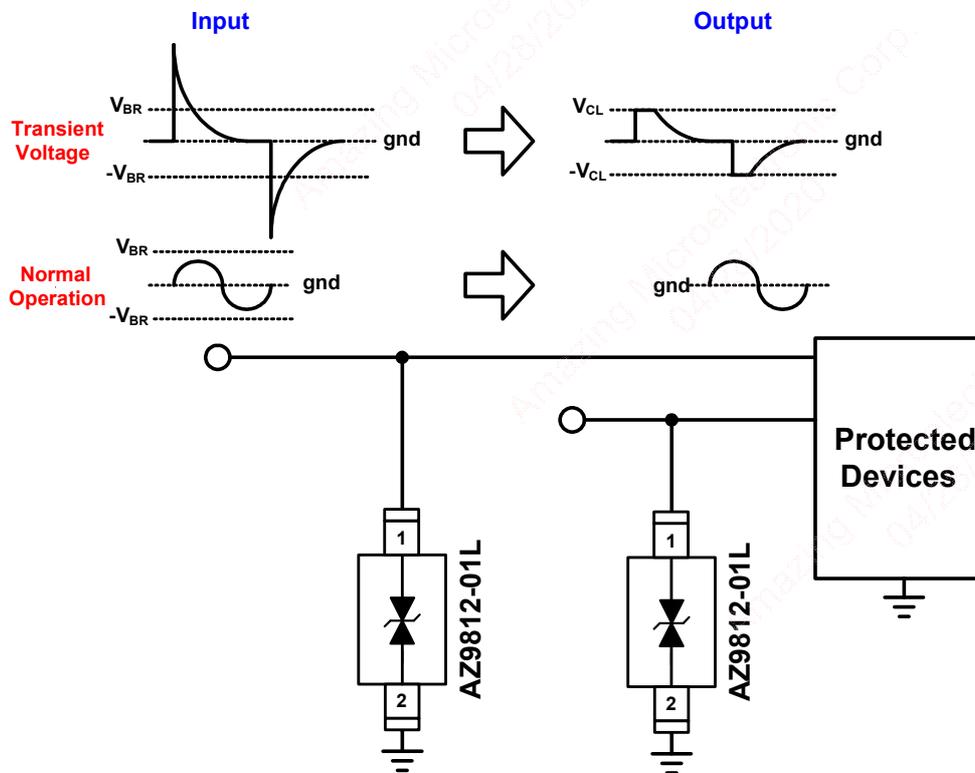


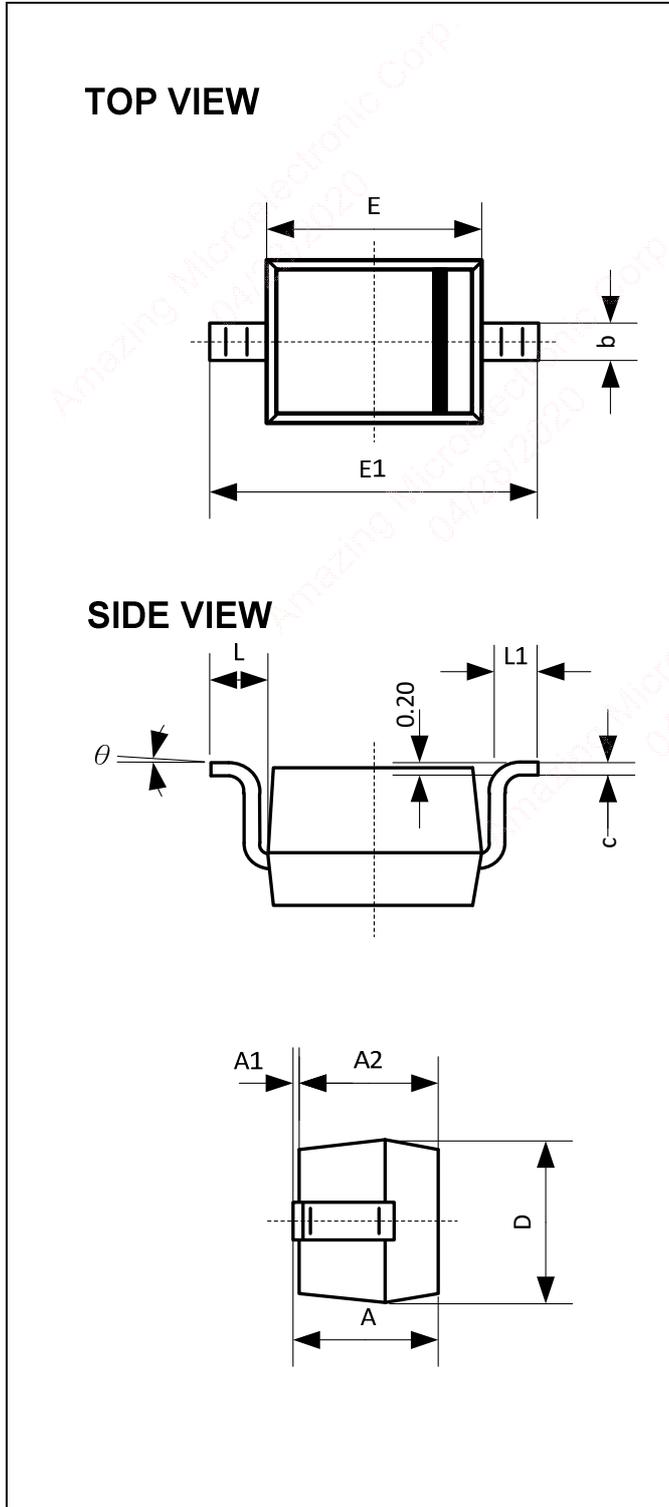
Fig. 1 ESD protection scheme by using AZ9812-01L.



## Mechanical Details

### SOD323-2L

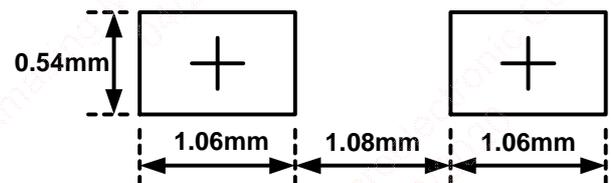
#### Package Diagrams



#### Package Dimensions

Symbol	Millimeters	
	Min.	Max.
A	0.80	1.00
A1	0.00	0.10
A2	0.80	0.90
b	0.25	0.35
c	0.08	0.15
D	1.20	1.40
E	1.60	1.80
E1	2.50	2.70
L	0.475REF	
L1	0.25	0.40
$\theta$	0	8

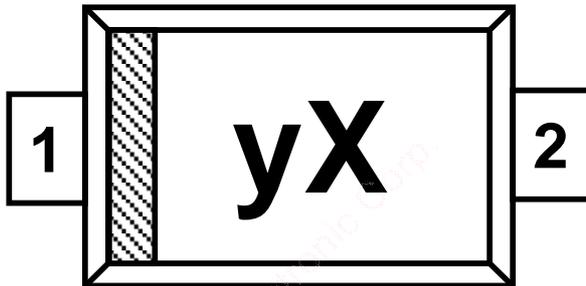
#### Land Layout



#### Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

### Marking Code



TOP View

y = Device Code  
X = Date Code

Part Number	Marking Code
AZ9812-01L.R7G (Green Part)	yX

Note. Green means Pb-free, RoHS, and Halogen free compliant.

### Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ9812-01L.R7G	Green	T/R	7 inch	3,000/reel	4 reels=12,000/box	6 boxes=72,000/carton

### Revision History

Revision	Modification Description
Revision 2020/04/28	Formal Release.