Features

- ESD Protect for 5 Lines with Unidirectional.
- Provide ESD protection for each line to
  IEC 61000-4-2 (ESD) ±16kV (air), ±10kV (contact)
  IEC 61000-4-4 (EFT) 35A (5/50ns)
  IEC 61000-4-5 (Lightning) 3.5 ~ 6A (8/20μs)
- For low operating voltage applications: 5V, 4.2V, 3.3V, and 2.5V etc.
- Fast turn-on and Low clamping voltage
- Array of surge rated equivalent TVS diodes
- Small package saves board space
- Solid-state silicon-avalanche and active circuit triggering technology
- Green part available

Applications

- Cellular Handsets and Accessories
- Small Panel Modules
- PDA's
- Portable Devices
- Digital Cameras
- Touch Panels
- Notebooks and Handhelds
- MP3 Players
- Peripherals

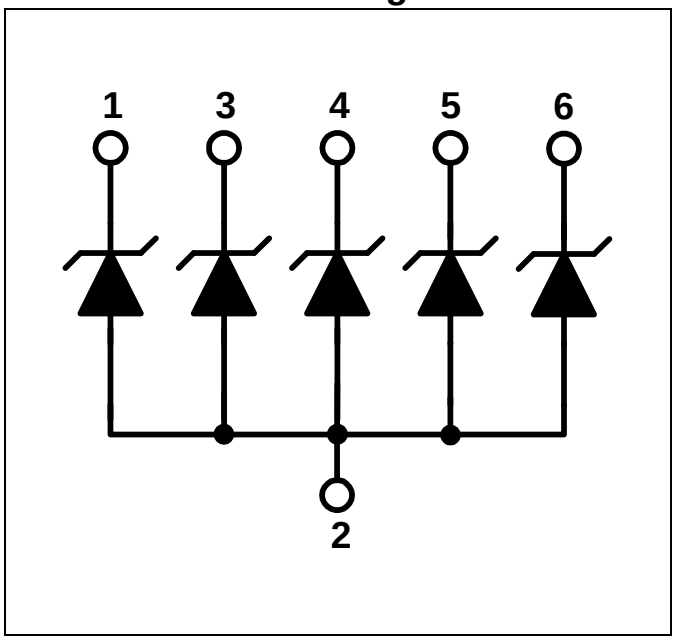
Description

AZ2115-05S is a design which includes surge rated clamping cell arrays to protect the power lines or data/control lines in an electronic systems. The AZ2115-05S has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

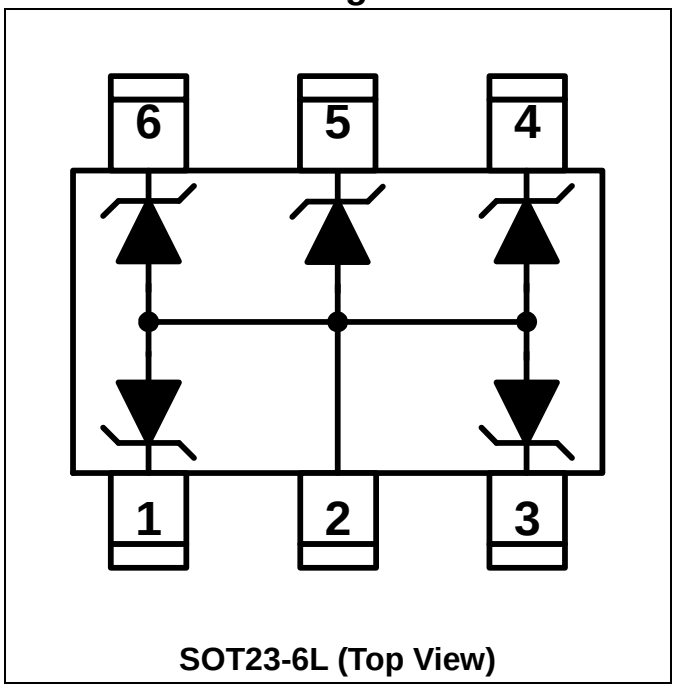
AZ2115-05S is a unique design which includes proprietary clamping cells in a single package. During transient conditions, the proprietary clamping cells prevent over-voltage on the power lines or control lines, protecting any downstream components.

AZ2115-05S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



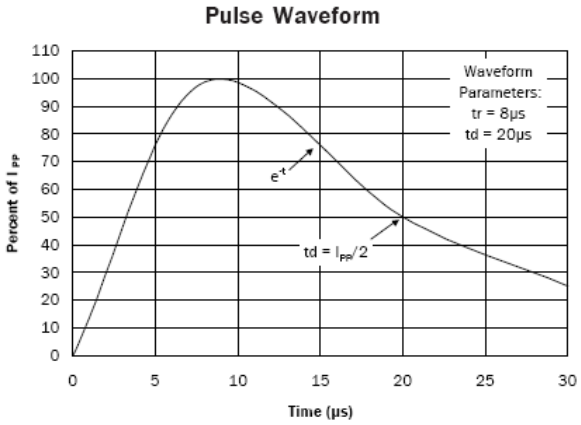
SOT23-6L (Top View)

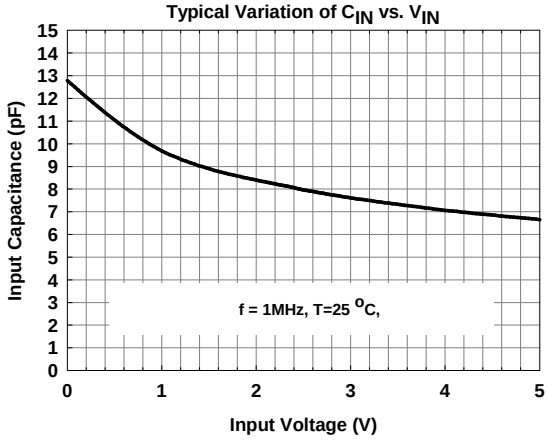
SPECIFICATIONS

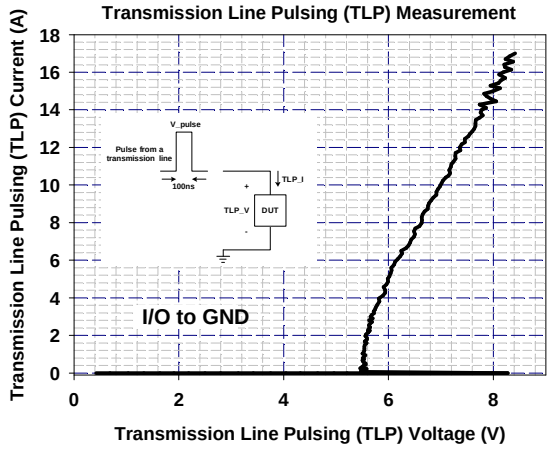
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20us)	I_{PP}	6 (pin-1, 3,4,6)	A
		3.5 (pin-5)	
Operating Supply Voltage (pin-1,-2 to pin-3)	V_{DC}	6	V
pin-1,-3, -4, -5, -6 to pin-2 ESD per IEC 61000-4-2 (Air)	V_{ESD-1}	16	kV
pin-1,-3, -4, -5, -6 to pin-2 ESD per IEC 61000-4-2 (Contact)		10	
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +85	°C
Storage Temperature	T_{STO}	-55 to +150	°C

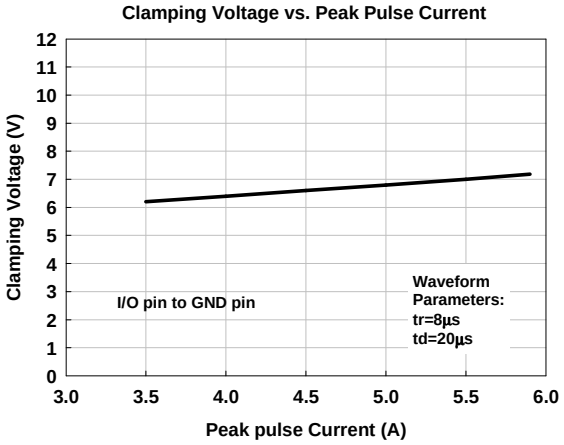
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MINI**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	pin-1,-3, -4, -5, -6 to pin-2, T=25 °C.			5	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = 5V, T=25 °C, pin-1,-3, -4, -5, -6 to pin-2.			2.5	µA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, pin-1,-3, -4, -5, -6 to pin-2	6		9	V
Forward Voltage	V_F	I_F = 15mA, T=25 °C, pin-2 to pin-1,-3, -4, -5, -6	0.6	0.8	1	V
Surge Clamping Voltage	$V_{CL-surge}$	I_{PP}=5A, tp=8/20us, T=25 °C, pin-1, -3, -4, -6 to pin-2.		6.8		V
		I_{PP}=3.5A, tp=8/20us, T=25 °C, pin-5 to pin-2.		6.2		
ESD Clamping Voltage	V_{clamp}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, pin-1,-3, -4, -5, -6 to pin-2.		8.5		**V**
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+6kV, T=25 °C, Contact mode, pin-1,-3, -4, -5, -6 to pin-2.		0.2		**Ω**
Channel Input Capacitance	C_{IN}	V_R= 0V, f = 1MHz, T=25 °C, pin-1,-3, -4, -5, -6 to pin-2.		13	15	pF

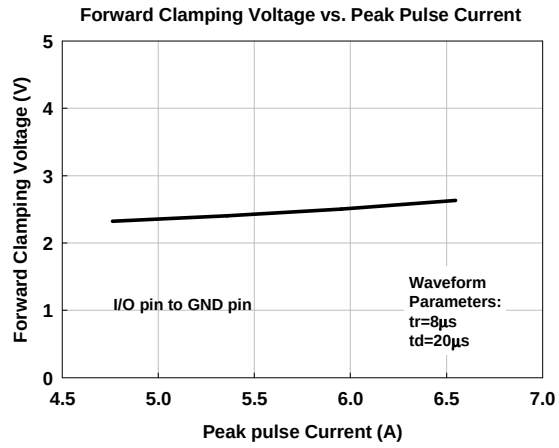
Typical Characteristics











Applications Information

The AZ2115-05S is designed to protect five lines against System ESD/EFT/Lightning pulses by clamping them to an acceptable reference.

The usage of the AZ2115-05S is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin 1, 3, 4, 5 and 6. The pin 2 should be connected directly to a ground plane on the board. All path lengths connected to the pins of AZ2115-05S should be kept as short as possible to minimize parasitic inductance in the board traces.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ2115-05S.
- Place the AZ2115-05S near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

Fig. 2 shows an example of PCB layout with the AZ2115-05S.

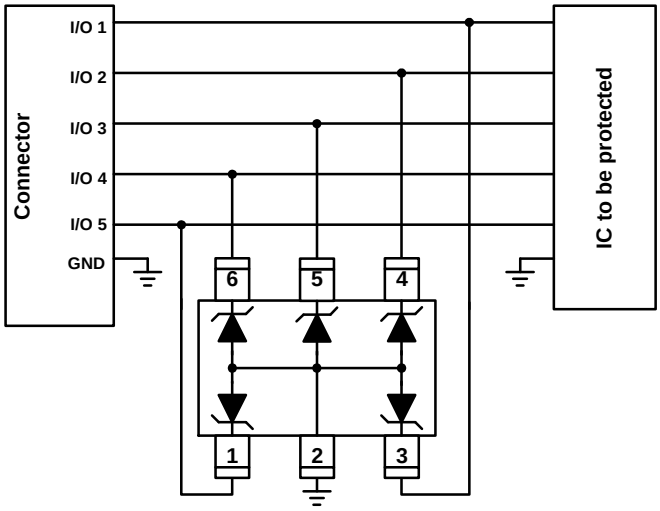


Fig. 1

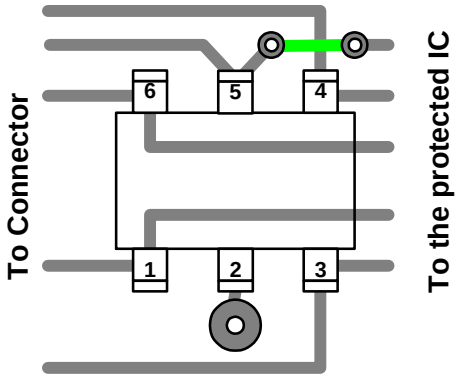


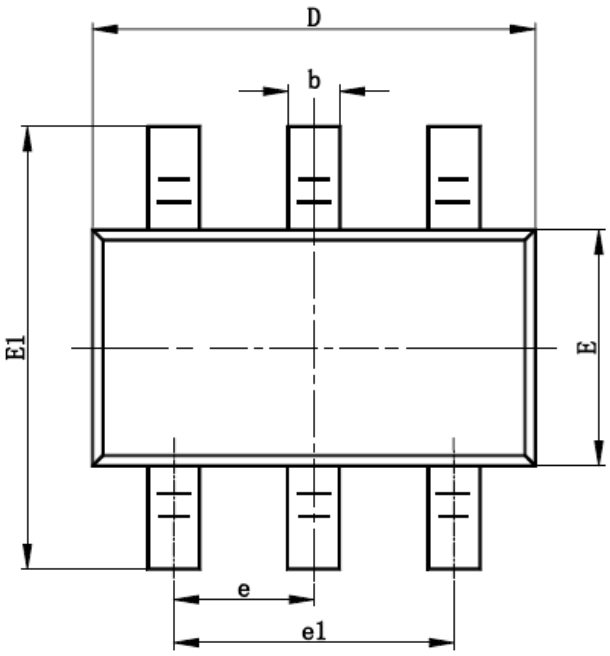
Fig. 2

Mechanical Details

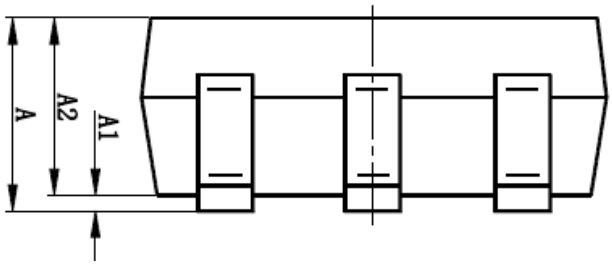
SOT23-6L

PACKAGE DIAGRAMS

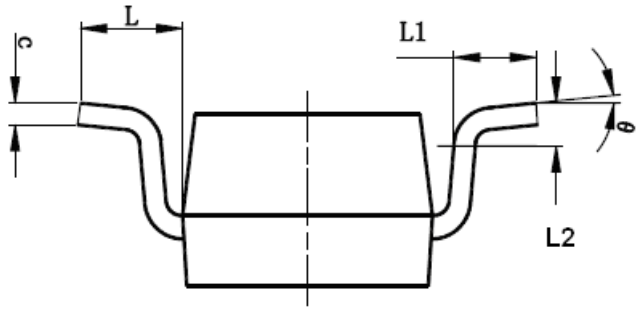
TOP VIEW



SIDE VIEW



END VIEW



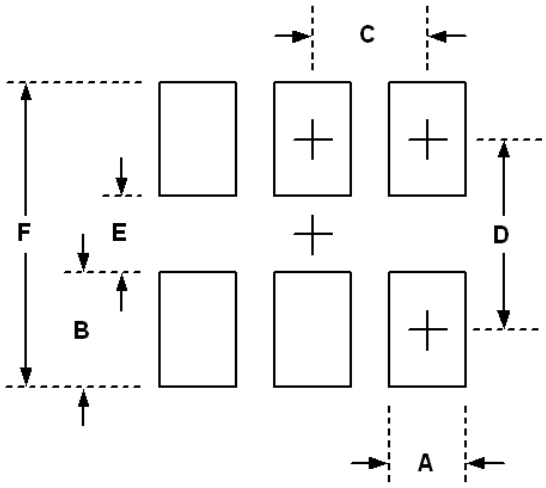
PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0	0.15	0.000	0.006
A2	0.9	1.3	0.035	0.051
b	0.3	0.5	0.012	0.020
c	0.08	0.21	0.003	0.008
D	2.72	3.12	0.107	0.123
E	1.4	1.8	0.055	0.071
E1	2.6	3	0.102	0.118
e	0.95BSC		0.037BSC	
e1	1.9BSC		0.075BSC	
L1	0.3	0.6	0.012	0.024
L	0.7REF		0.028REF	
L2	0.25BSC		0.010BSC	
θ	0	8	0	8

Notes:

- This dimension complies with JEDEC outline standard MO-178 Variation AB.
- Dimensioning and tolerancing per ASME Y14.5M-1994.
- All dimensions are in millimeters, and the dimensions in inches are for reference only.
- 1mm = 40 mils = 0.04 inches.

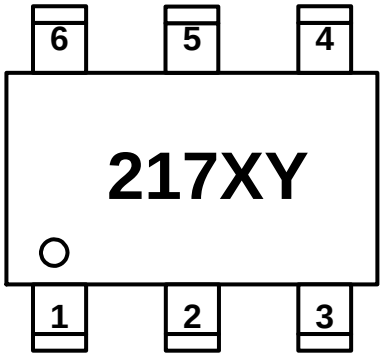
LAND LAYOUT



Dimensions		
Index	**Millimeter**	**Inches**
A	0.52~0.60	0.0205~0.024
B	1.10	0.043
C	0.95	0.037
D	2.50	0.098
E	1.40	0.055
F	3.60	0.141

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



Part Number	Marking Code
AZ2115-05S	217XY
AZ2115-05S (Green part)	**225XY**

217 = Device Code
X = Date Code
Y = Control Code

Ordering Information

PN#	Material	Type	Reel size	MOQ/interal box	MOQ/carton
AZ2115-05S.R7G	Green	T/R	7 inch	4 reel=12,000/box	6 box=72,000/carton

Revision History

Revision	Modification Description
Revision 2008/03/28	Original Formal Release.
Revision 2008/09/29	Add the marking code for Green part.
Revision 2008/12/26	Update the PACKAGE DIMENSIONS.
Revision 2011/06/18	1. Update the Company Logo. 2. Add the Ordering Information.